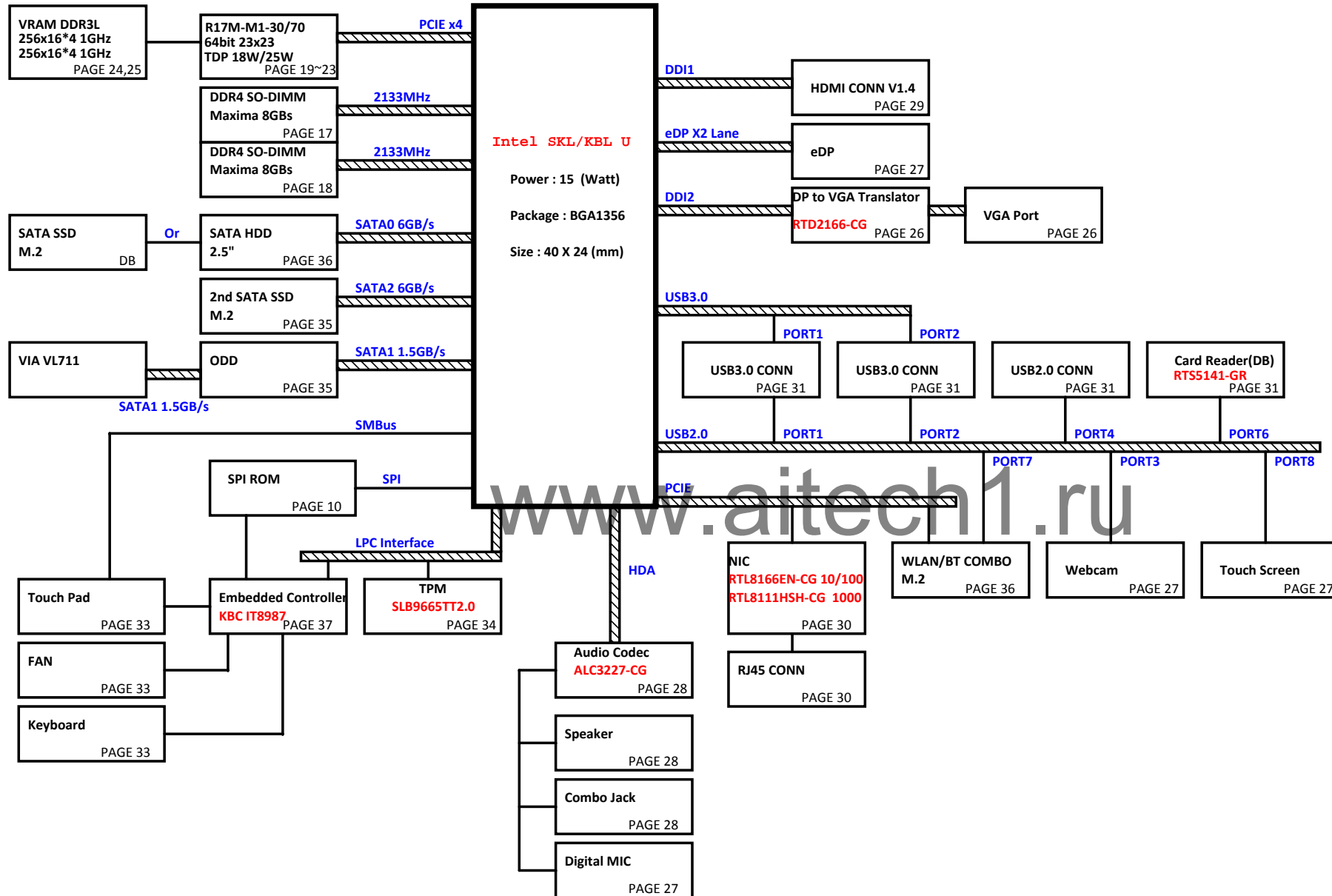


Intel SKL-U/KBL-U Platform Block Diagram

01



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

+3V <4,10,11,12,13,14,15,17,18,26,27,28,29,30,31,33,34,35,37,43,45>
+1.0V <4,37,42,43>
+VCCSTPLL <4,5,6,9,42>

HDMI

<29> IN_D2# IN_D2# E55
<29> IN_D2 IN_D2 F55
<29> IN_D1# IN_D1# F58
<29> IN_D1 IN_D1 F58
<29> IN_D0# IN_D0# F53
<29> IN_D0 IN_D0 G53
<29> IN_CLK# IN_CLK# F56
<29> IN_CLK IN_CLK G56

<26> DD11_TX0_N DD11_TX0_N D50
<26> DD11_TX0_P DD11_TX0_P D50
<26> DD11_TX1_N DD11_TX1_N D52
<26> DD11_TX1_P DD11_TX1_P D52

SI

<29> SDVO_CLK SDVO_CLK L13
<29> SDVO_DATA SDVO_DATA L12
+3V R9055 DDPC_CTRLDATA
2.2K_4
TP3 1DDPD_CTRLDATA
+VCCIO R3 24.9_1%_4 EDP_RCOMP

eDP_COMPIO and ICOMPIO signals should be shorted near balls and routed with typical impedance <25 mohms

U1A SKL_ULT ? Need apply PN

DDI1_TXN[0] DDI1_TXP[0]
DDI1_TXN[1] DDI1_TXP[1]
DDI1_TXN[2] DDI1_TXP[2]
DDI1_TXN[3] DDI1_TXP[3]
DDI2_TXN[0] DDI2_TXP[0]
DDI2_TXN[1] DDI2_TXP[1]
DDI2_TXN[2] DDI2_TXP[2]
DDI2_TXN[3] DDI2_TXP[3]

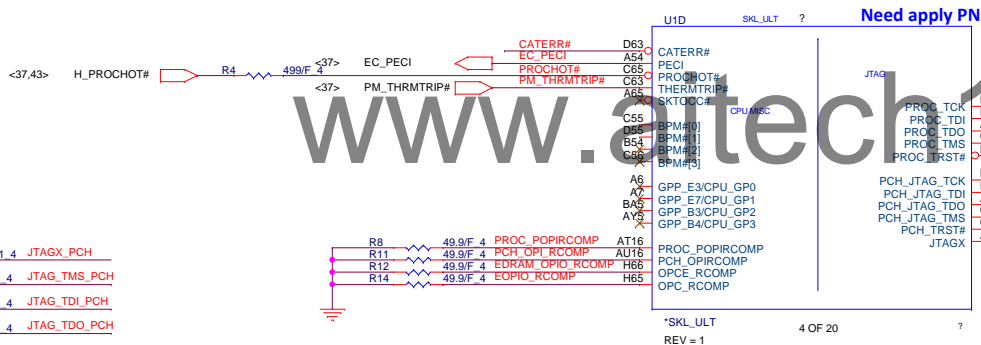
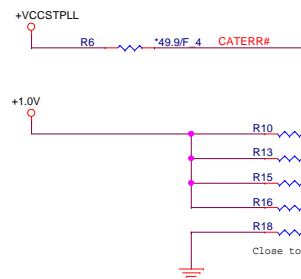
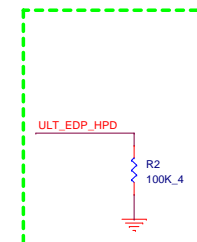
DISPLAY SIDEBANDS

*SKL_ULT
REV = 1

1 OF 20

EDP_TXN[0] EDP_TXP[0]
EDP_TXN[1] EDP_TXP[1]
EDP_TXN[2] EDP_TXP[2]
EDP_TXN[3] EDP_TXP[3]
EDP_AUXN EDP_AUXP
EDP_DISP_UTIL
DDI1_AUXN DDI1_AUXP
DDI2_AUXN DDI2_AUXP
DDI3_AUXN
HDMI_HPD_CON DDI1_HPD_CON
ULT_EDP_HPD
PCH_LVDS_BLON PCH_DPST_PWM
PCH_DISP_ON

Reserve EDP_HPD opposites circuit!



*SKL_ULT
REV = 1

4 OF 20

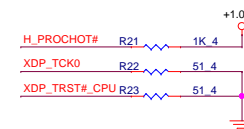
XDP_TRST#_CPU R863 0.4/\$PROC_TEST#

Close to EC

PM_THRMTRIP# R5 1K_4
Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL.
470 OHM IS FOR I/P

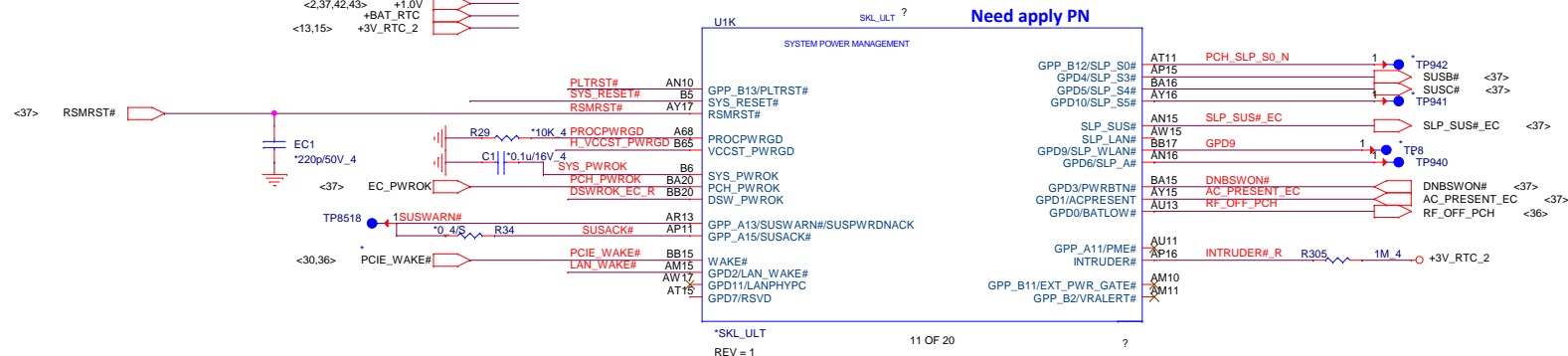
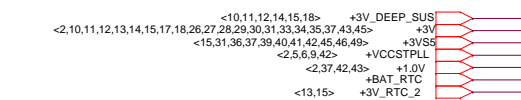
PLACE NEAR CPU

XDP_TMS_CPU R17 51_4
XDP_TDI_CPU R19 51_4
XDP_TDO_CPU R20 51_4

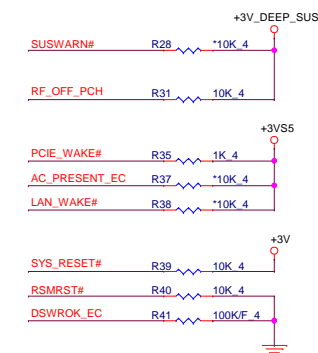


PROJECT : 0P1B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	02 - SKYPAKE 1/15 (eDP/DDI)	1A
Date: Wednesday, March 08, 2017	Sheet 2 of 51	



PCH Pull-high/low(CLG)

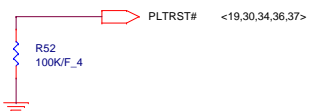


For DS3 Sequence

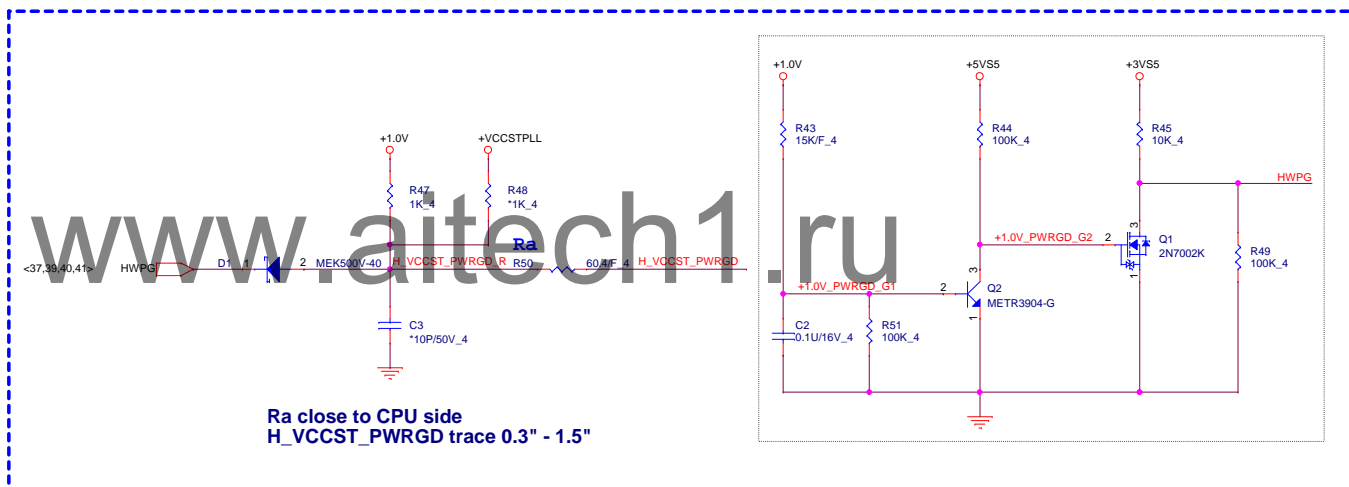


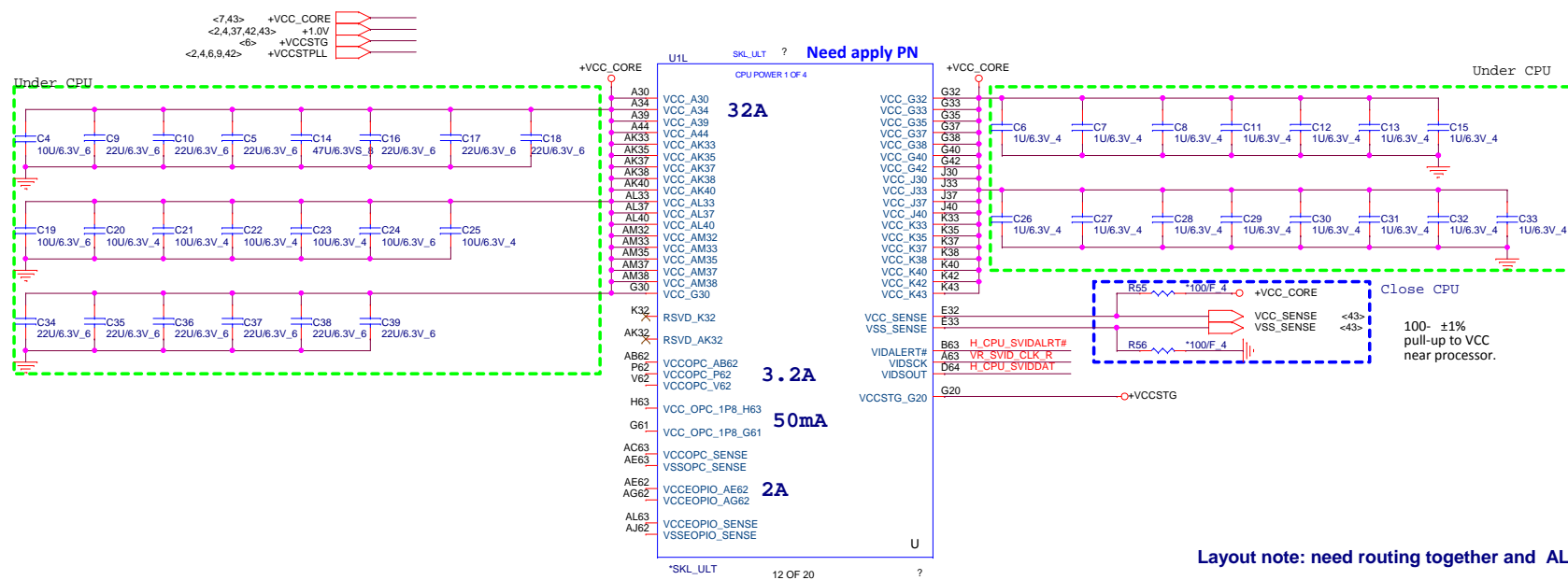
PLTRST#(CLG)

Check Rise/Fall time less than 100ns

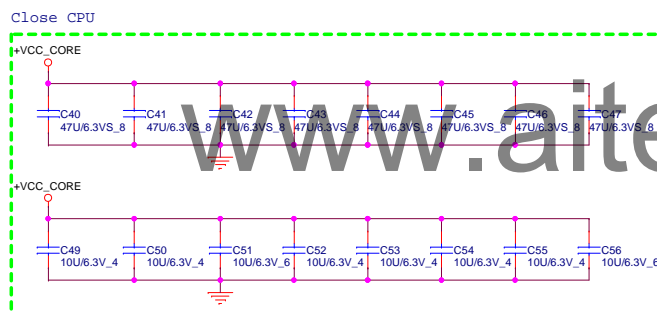


System PWR_OK(CLG)

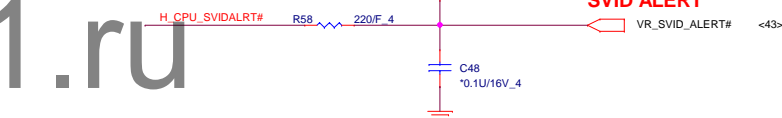




Layout note: need routing together and ALERT need between CLK and DATA.



CLOSE TO CPU
PLACE THE PU RESISTORS



PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE



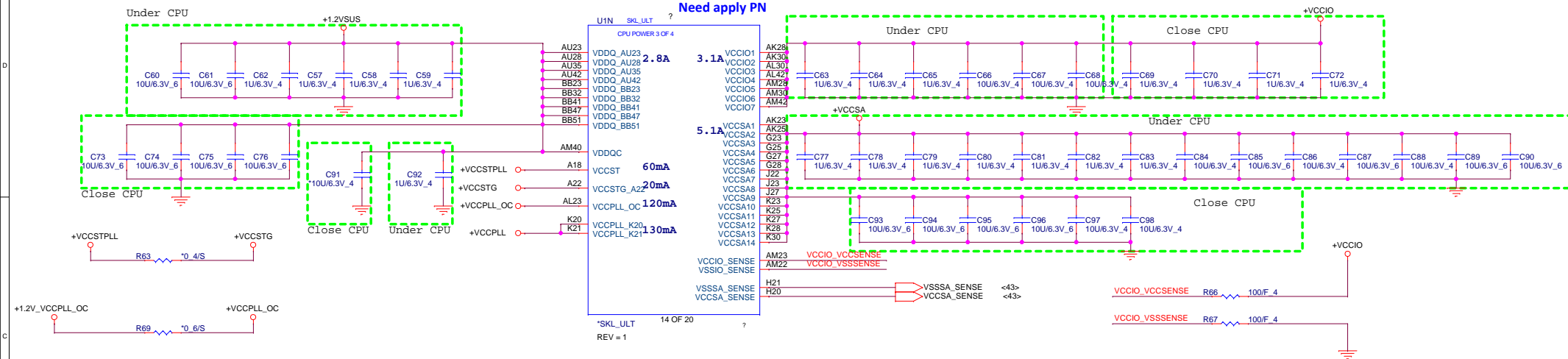
CLOSE TO CPU
PLACE THE PU RESISTORS



Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

+VCCSTPLL <2,4,5,9,42>
 +VCCSA <43,44>
 +1.2VSUS <3,17,18,40,42>
 +1.0V_DEEP_SUS <9,13,15,41,42>
 +1.0V <2,4,37,42,43>
 +3VPCU <13,31,33,36,37,38,39>

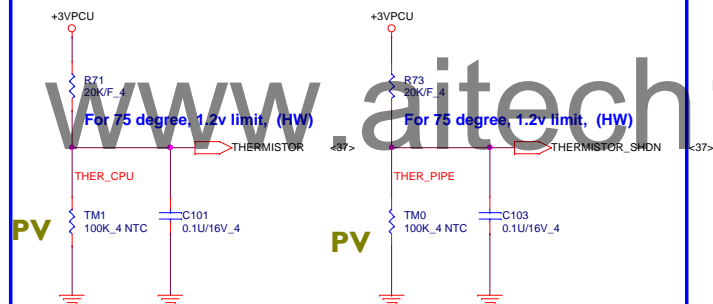
Need apply PN



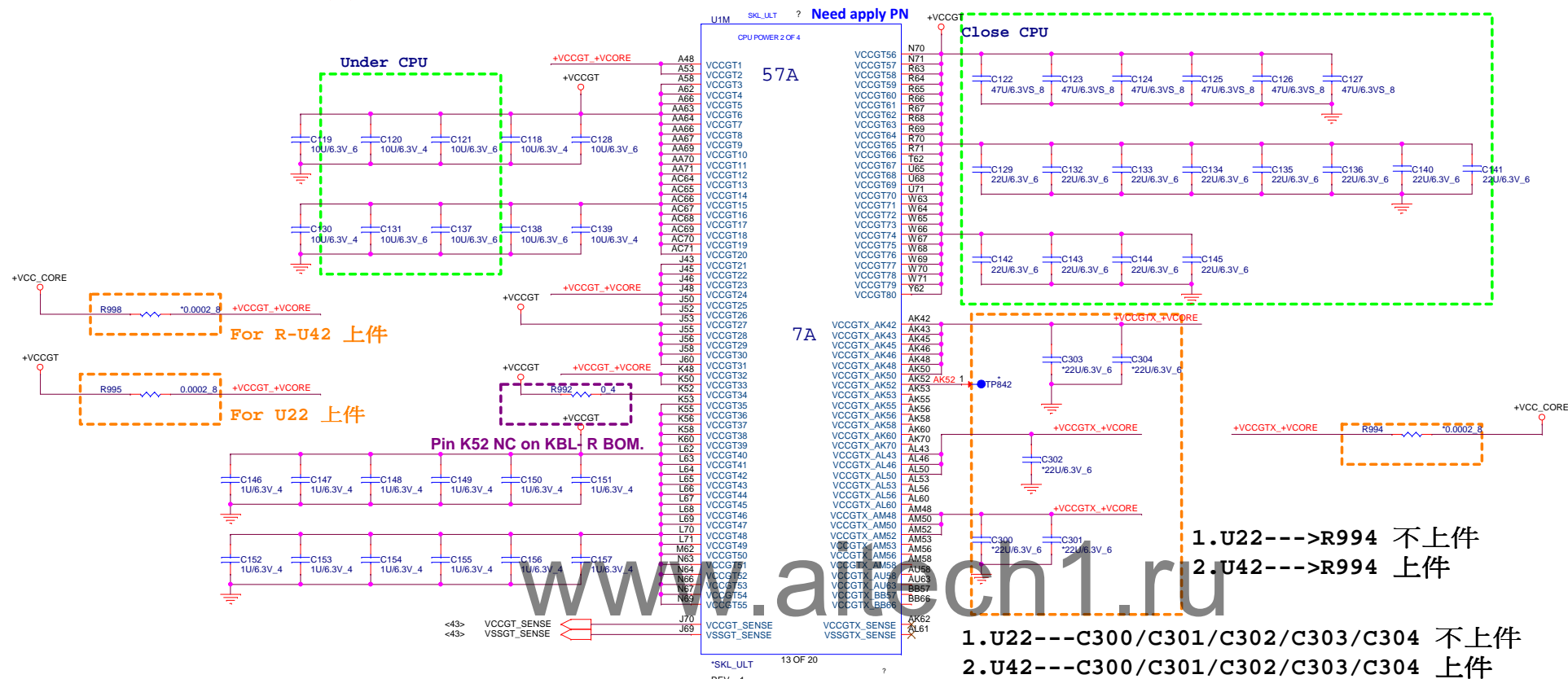
IO Thrm Protect

For 75 degree, 1.2v limit, (HW)

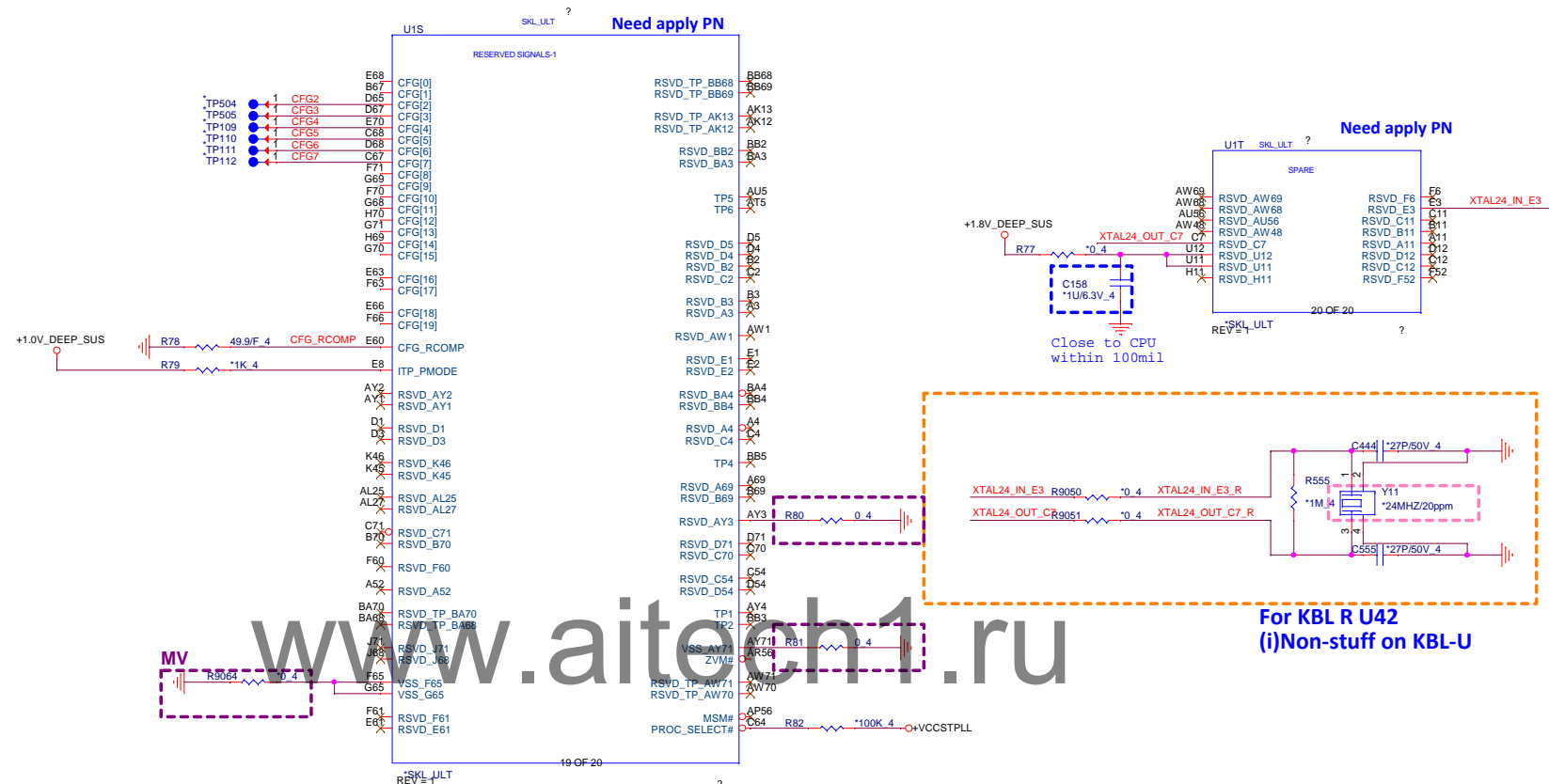
For 75 degree, 1.2v limit, (HW)



Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCeOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



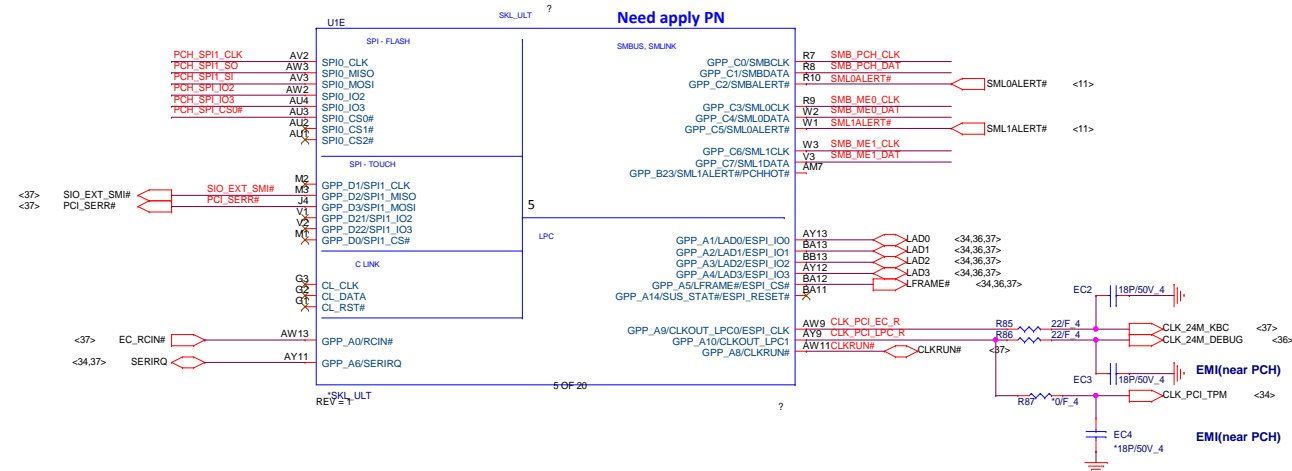
Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



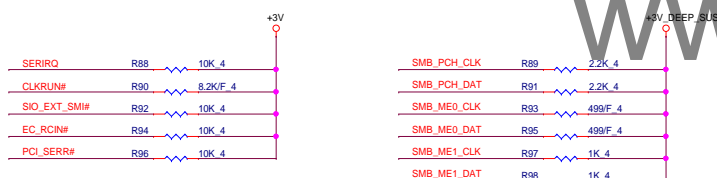
Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R83 *1K 4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R84 1K 4

+3V_DEEP_SUS <4,11,12,14,15,18>
 +3V <2,4,11,12,13,14,15,17,18,26,27,28,29,30,31,33,34,35,37,43,45>
 +5V <26,27,28,29,33,35,36,45>
 +1.0V <2,4,37,42,43>
 +3VSS <4,15,31,36,37,39,40,41,42,45,46,49>



GPIO Pull UP



PCH SPI ROM(CLG)

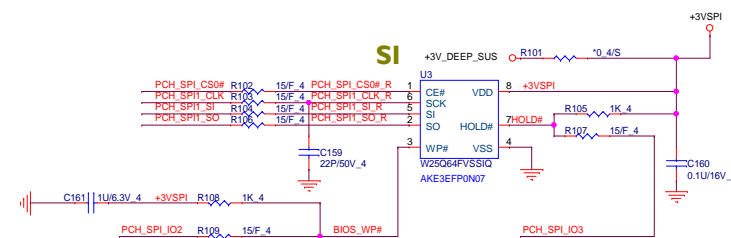
Vender	Size	P/N
EON	8MB	AKE3EZNOQ01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EPF0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGNOQ01 (GD25B64BSIGR)
Socket		DFHS08FS023

<37> PCH_SPI_CS0#_R
 <37> PCH_SPI_CLK_R
 <37> PCH_SPI_SI_R
 <37> PCH_SPI_SO_R

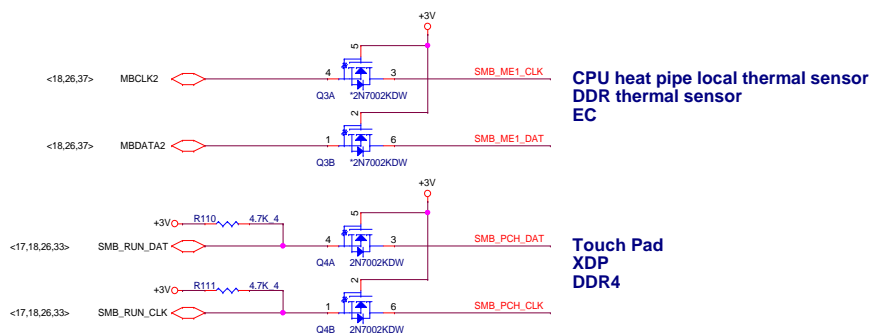
need place to TOP

TP17 1 PCH_SPI_CS0#_R
 TP18 1 PCH_SPI_CLK_R
 TP19 1 PCH_SPI_SI_R
 TP20 1 PCH_SPI_SO_R
 TP21 1 BIOS_WP#
 TP22 1 HOLD#

PCH SPI ROM(CLG)

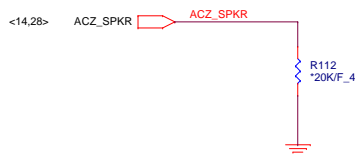


SMBus/Pull-up(CLG)

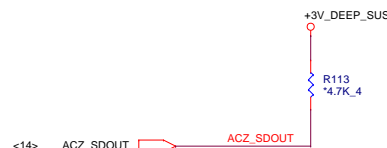


Functional Strap Definitions

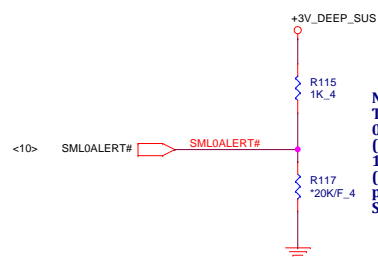
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



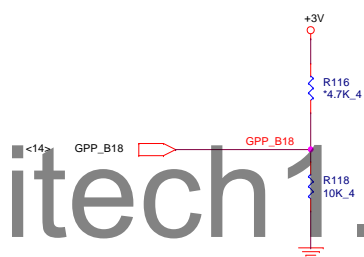
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



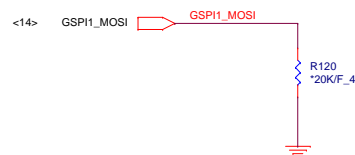
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



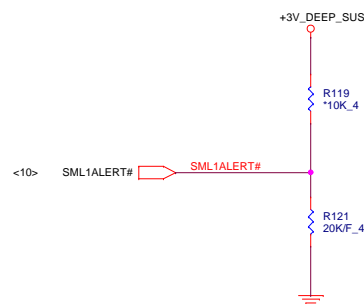
No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



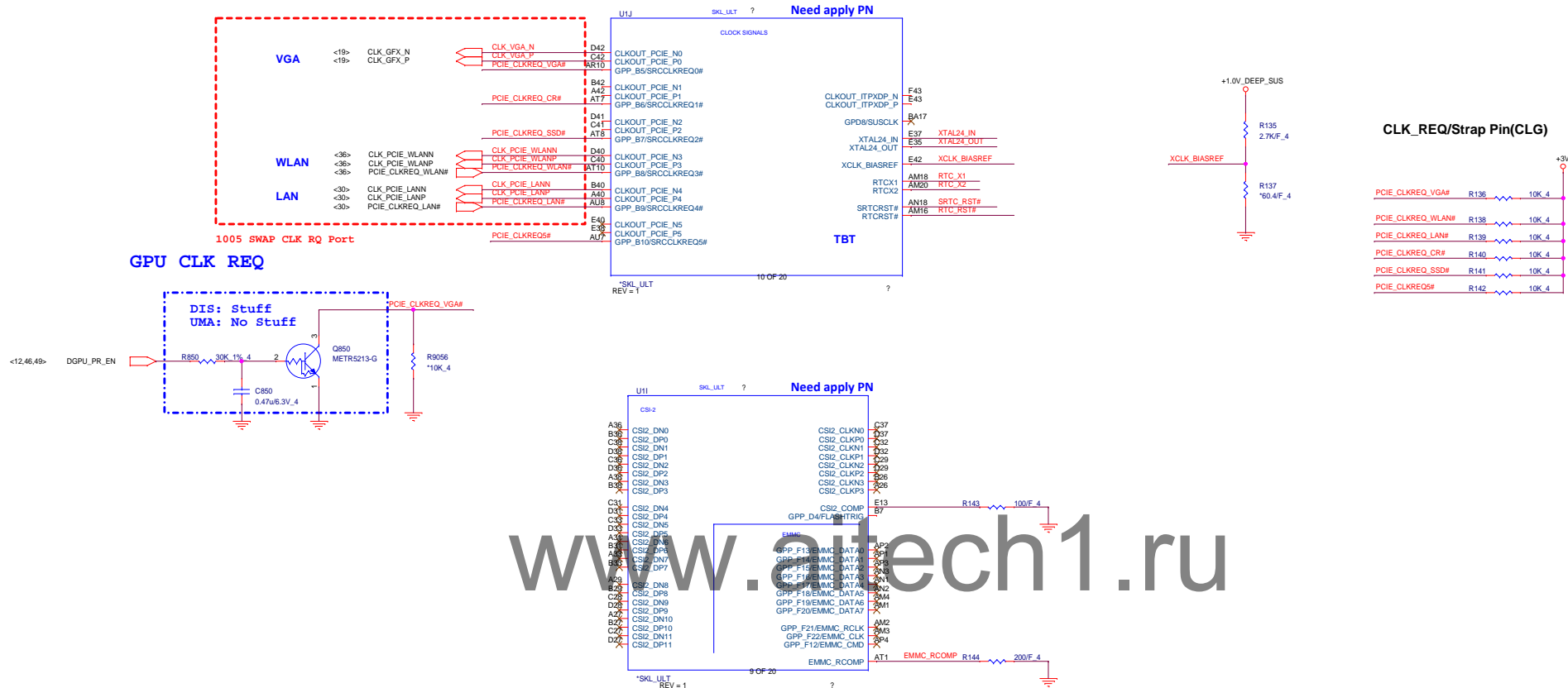
No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



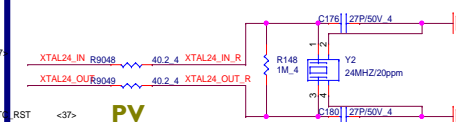
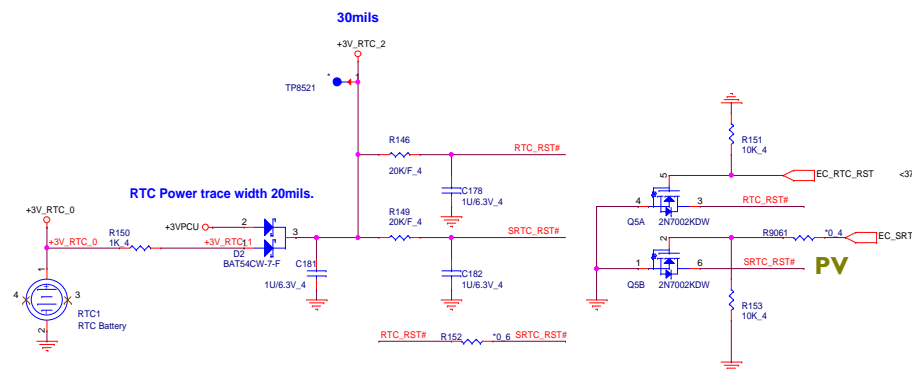
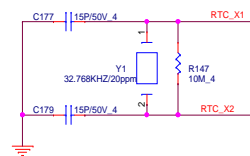
No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.
Bit 10 Boot BIOS Destination
0 SPI
1 LPC



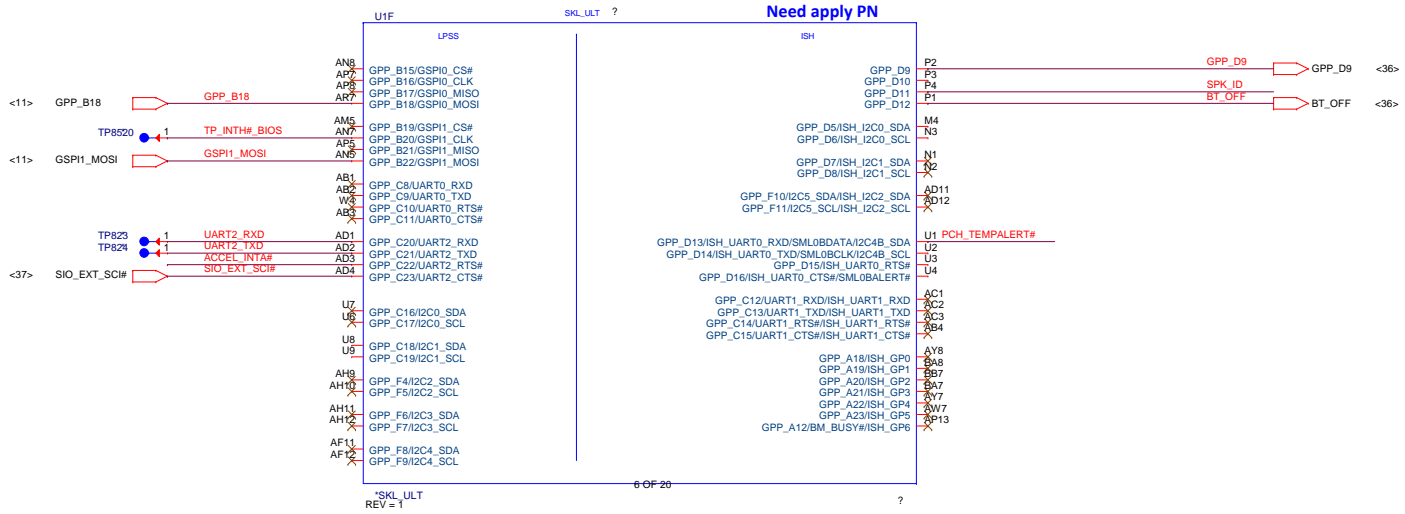
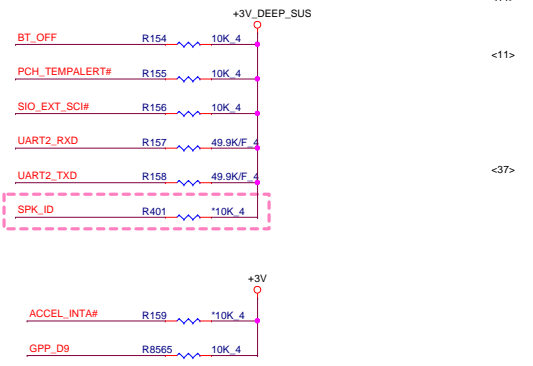
No Boot:
The signal has a weak internal pull-down.
0 = LPC is selected for EC.
1 = eSPI is selected for EC.



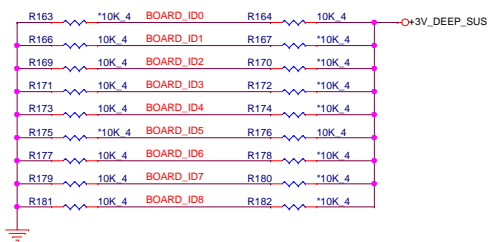
The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.



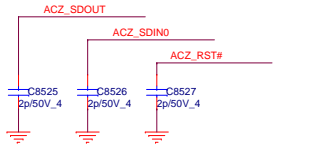
Skylake (GPIO)



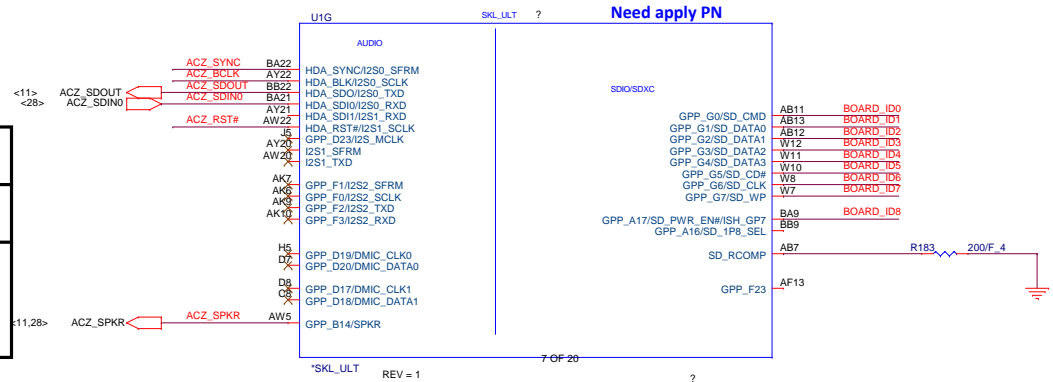
HDA Bus(CLG)




www.aitech1.ru



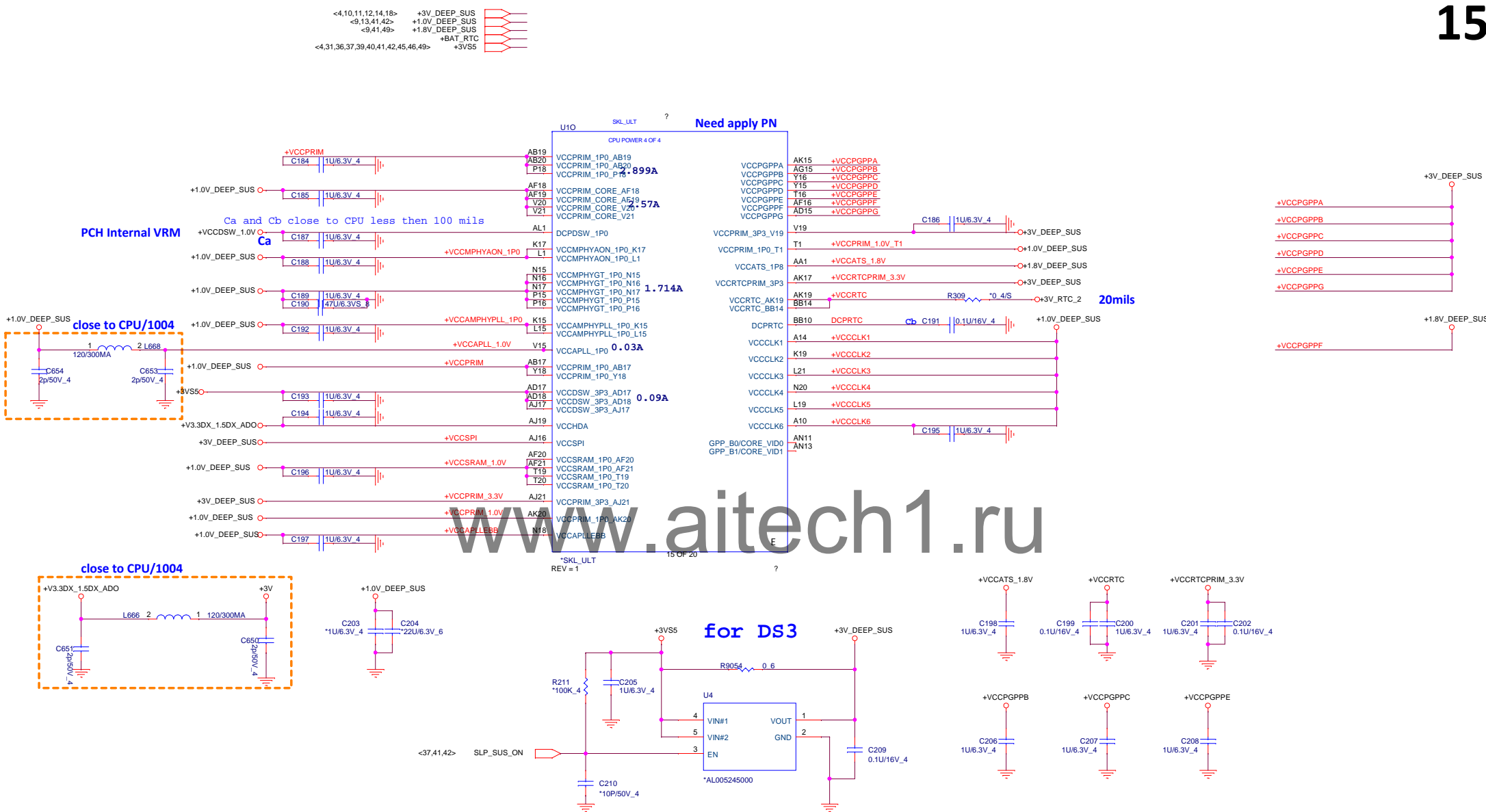
skylake	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4:3]	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7	ID6 ID5	ID4 ID3	ID2 ID1	ID0
Definition	Reserve (Default = 00)	00 SKL U 01 KBL U 10 Base U 11 KBL R(4+2)	Reserve (Default = 00)	00 14" 01 15" 10 Reserve 11 Reserve	0 : UMA 1 : DIS






PROJECT : 0P1B
Quanta Computer Inc.

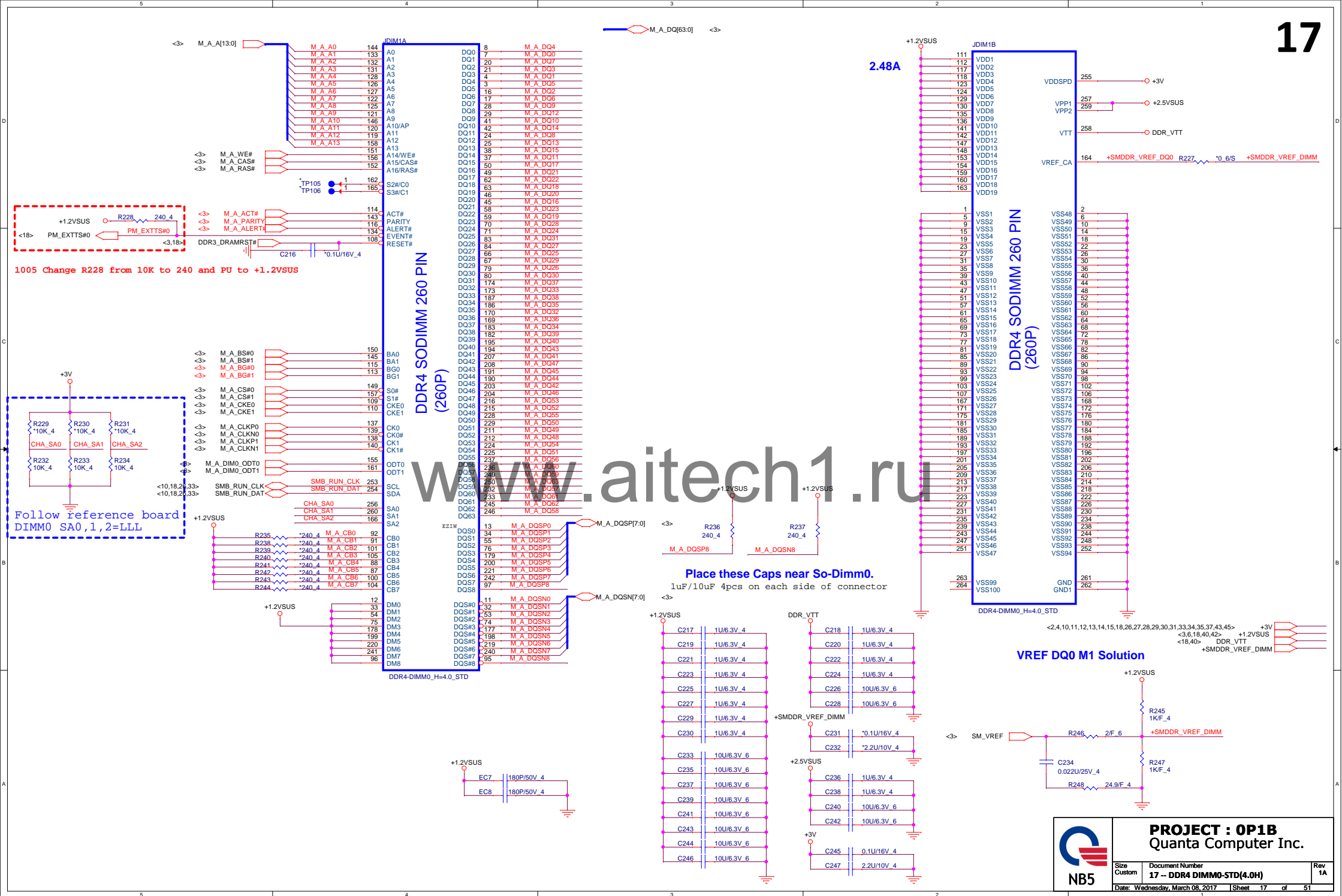
Size Custom	Document Number 14 - SKYLAKE 13/15 (GPIO)	Rev 1A
Date: Wednesday, March 08, 2017		Sheet 14 of 51



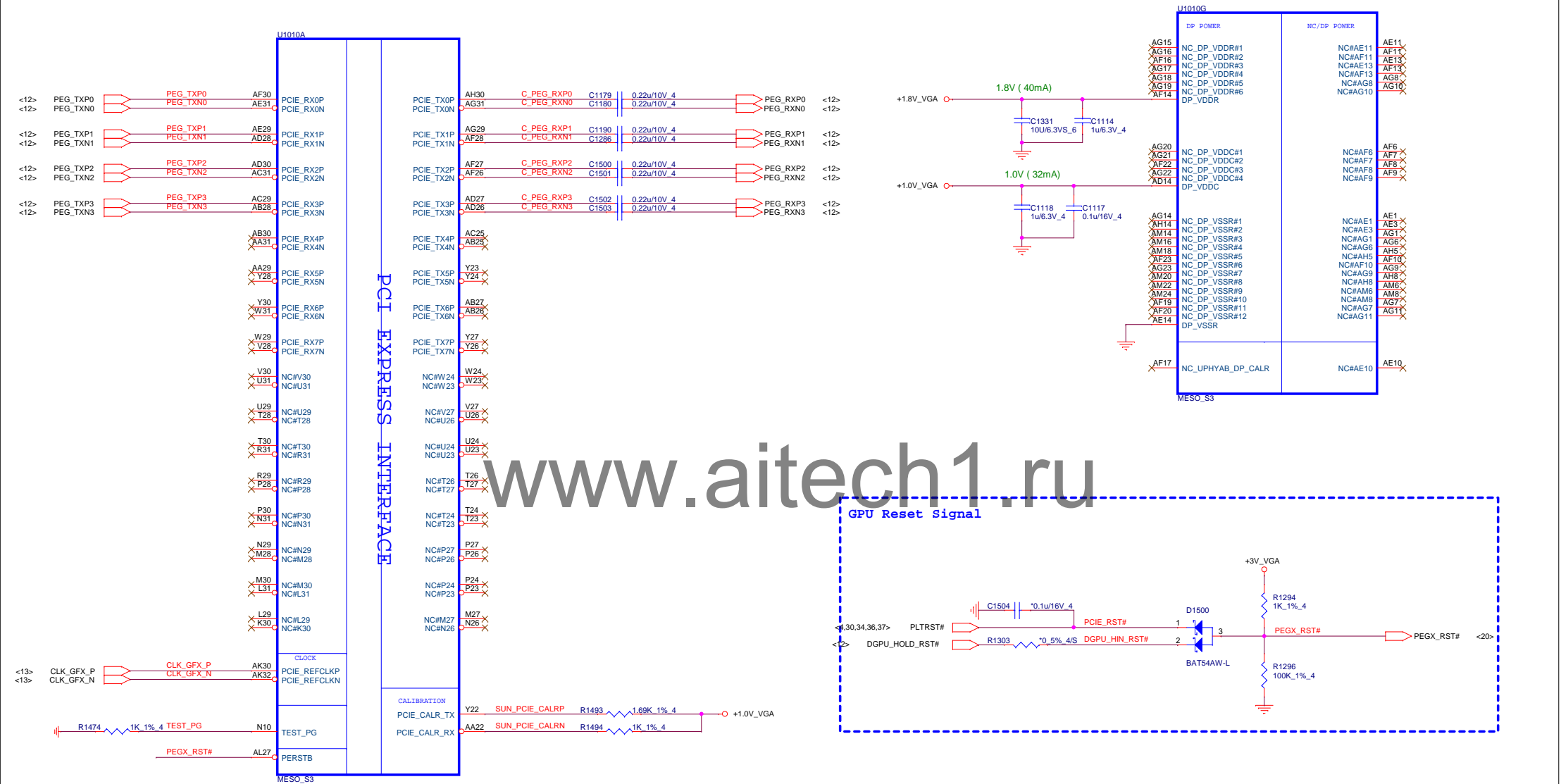
www.aitech1.ru

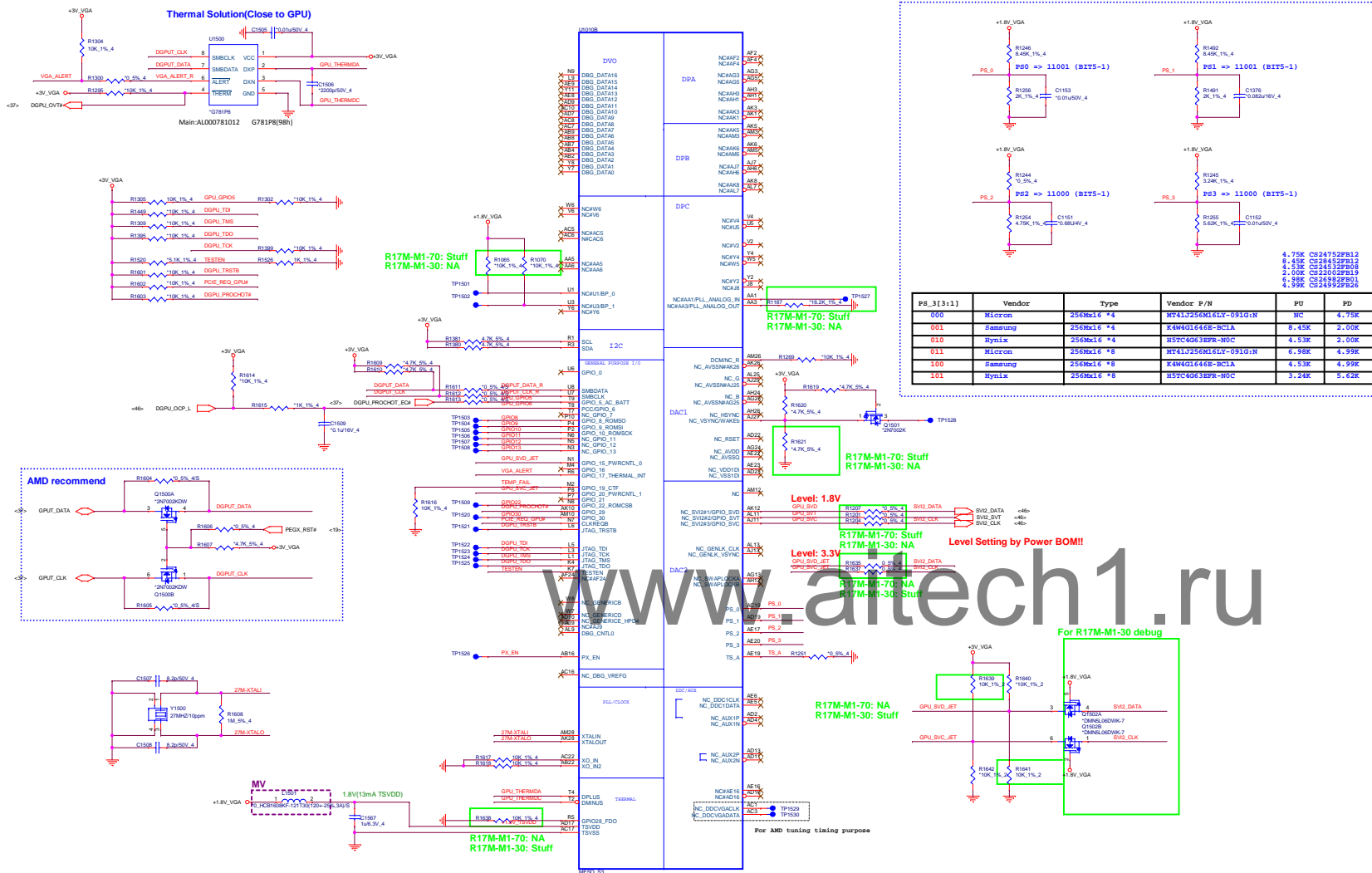
del XDP

 NB5	PROJECT : 0P1B Quanta Computer Inc.		
	Size	Document Number	Rev
		16 -- SKYLAKE 15/15 XDP&APS *	1A
Date: Wednesday, March 08, 2017 Sheet 16 of 51			









- MLPS Implementation**
- Connect GPD_28 to 10K pull-down to enable MLPS
 - If any of PS_0/2/3 is not used, leave "No connect"
 - PS pin, R, pd and C must be properly populated per tables below
 - Place MLPS circuit components as close to the ASIC as possible
 - Total DC resistance of trace between PS pin and C should be less than 2 ohms
 - Total DC resistance of trace between C and ground should be less than 2 ohms
 - Trace capacitance should be less than 10pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table	
C (pF)	Bits(5,4)
680	00
82	01
10	10
NC	11

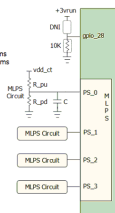
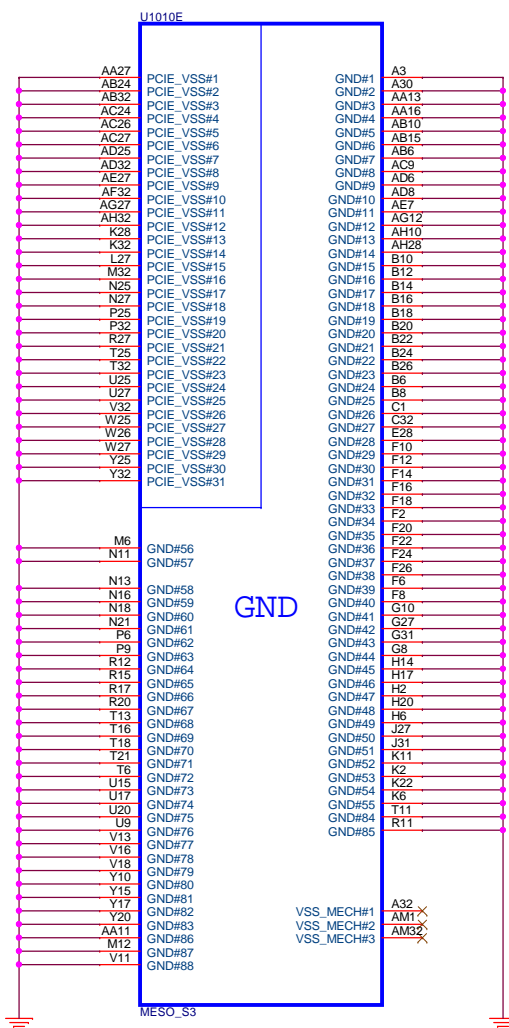


Table 3-24 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

MLPS bit	Strap Name	Description	Recommended Settings
PS_0[11]	ROM_CONFIG[0]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[0] follows the ROM type.	Design dependent, see the description.
PS_0[12]	ROM_CONFIG[1]	If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[1] defines the primary memory aperture size. See Primary Memory Aperture Size (p. 21).	Design dependent, see the description.
PS_0[13]	ROM_CONFIG[2]	If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2] defines the primary memory aperture size. See Primary Memory Aperture Size (p. 21).	Design dependent, see the description.
PS_0[14]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[15]	N/A	Reserved.	1
PS_1[11]	STRAP_BIF_GEN3_EN_A	PCIE GEN3 capability. 1 = PCIE GEN3 is supported. 0 = PCIE GEN3 is not supported.	Design dependent, see the description.
PS_1[12]	STRAP_BIF_CLK_PEN	Determines whether or not the PCIe reference clock provided in the PCI configuration space (otherwise known as CLKREQ#). 0 = The CLKREQ# power management capability is disabled. 1 = The CLKREQ# power management capability is enabled. Reserved for internal use only. Must be 0 at reset.	0
PS_1[13]	N/A	Reserved.	0
PS_1[14]	STRAP_TX_CPS_DRV_FULL_SWING	Control the transmitter full-half swing mode. 0 = The transmitter half-swing is enabled. 1 = The transmitter full-swing is enabled.	1
PS_1[15]	STRAP_TX_DEEN_PEN	PCI EXPRESS transmitter de-emphasis enable. 0 = Tx de-emphasis disabled. 1 = Tx de-emphasis enabled.	Design dependent, see the description.
PS_2[11]	N/A	Reserved.	0
PS_2[12]	N/A	Reserved.	0
PS_2[13]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2[14]	N/A	Reserved.	1
PS_2[15]	N/A	Reserved.	1
PS_3[11]	BOARD_CONFIG[0]	Board configuration related information, such as memory ID.	Design dependent, see the description.
PS_3[12]	BOARD_CONFIG[1]	Board configuration related information, such as memory ID.	Design dependent, see the description.
PS_3[13]	N/A	Reserved.	1
PS_3[14]	N/A	Reserved.	1
PS_3[15]	N/A	Reserved.	1



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS **ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET**

RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1= INSTALL 3K RESISTOR
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

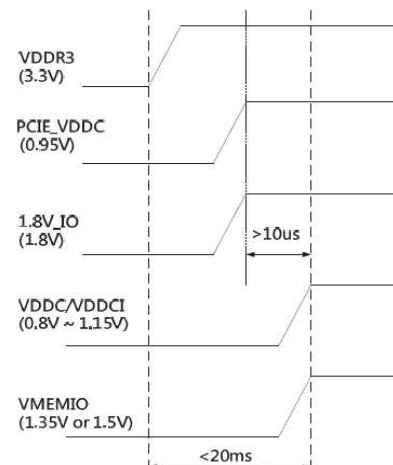
NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

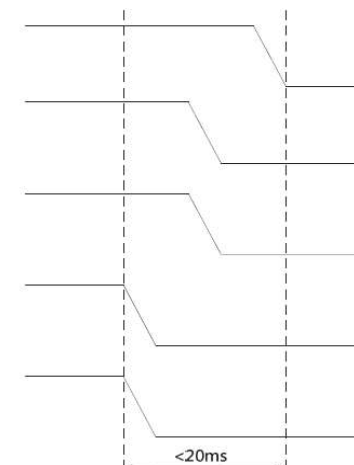
GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE

POWER UP

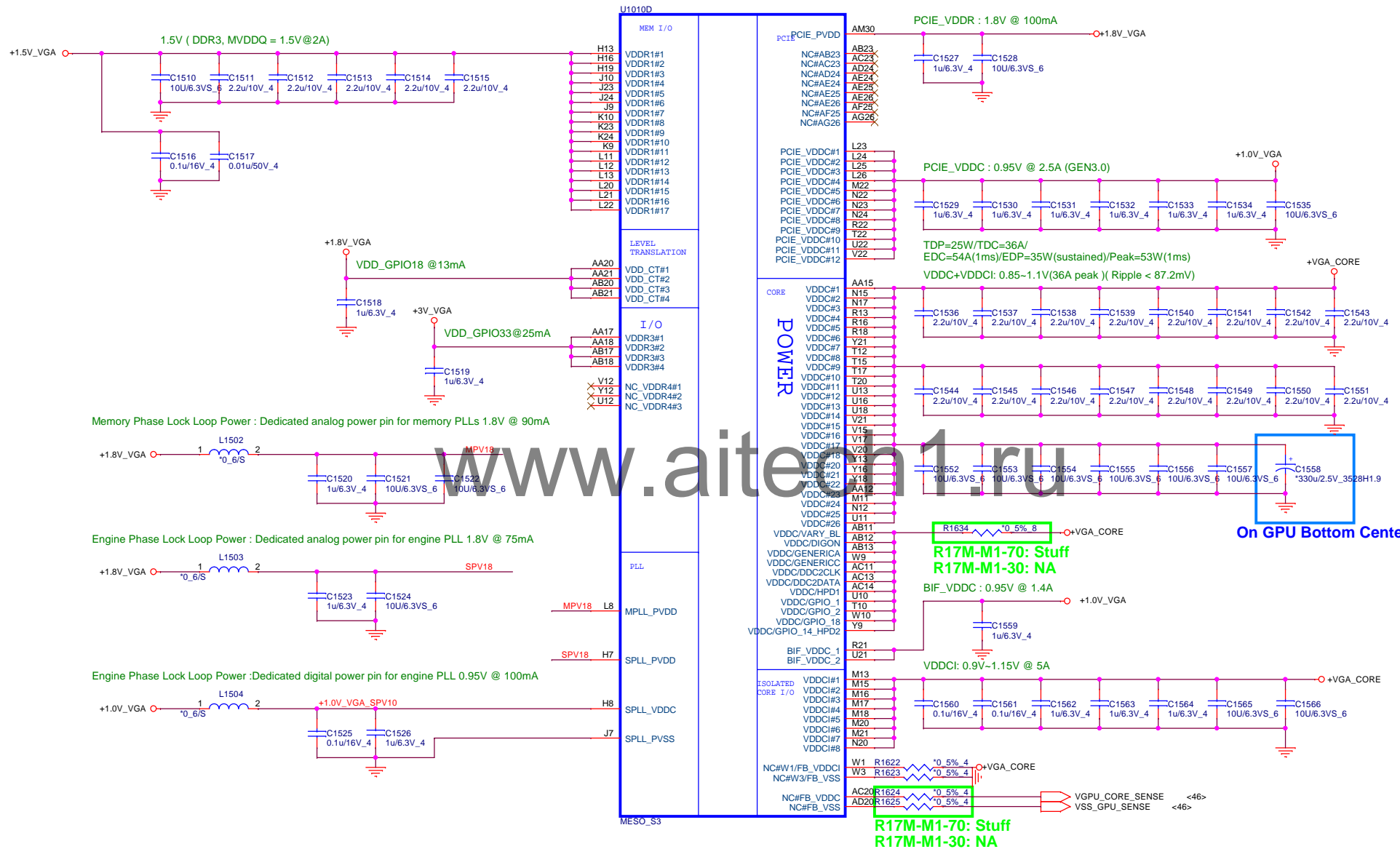


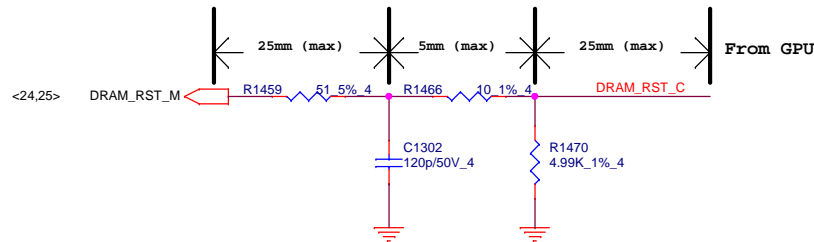
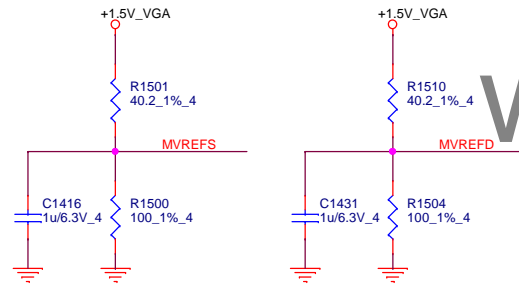
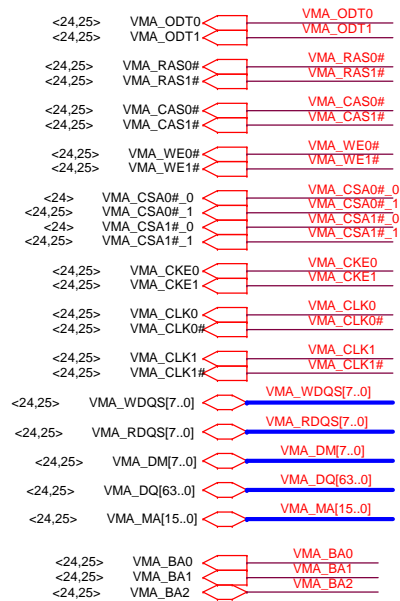
POWER DOWN



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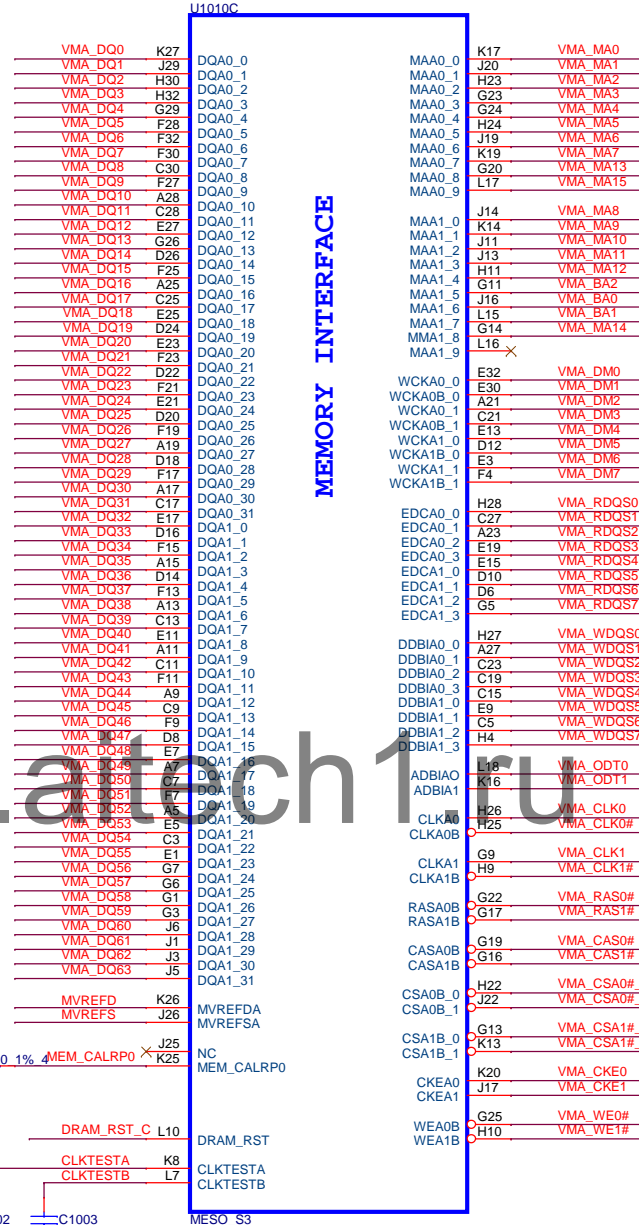
Size	Document Number	Rev
	M1-70_S3_GND/LVDS/Strap	100
Date:	Wednesday, March 08, 2017	Sheet 21 of 51





Place all these components very close to GPU. (Within 25mm)
Keep all component close to each Other. (within 5mm)

This basic topology should be used for DRAM_RST for DDR3/GDDR5.

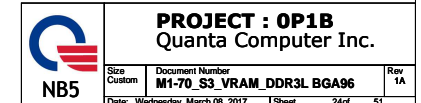


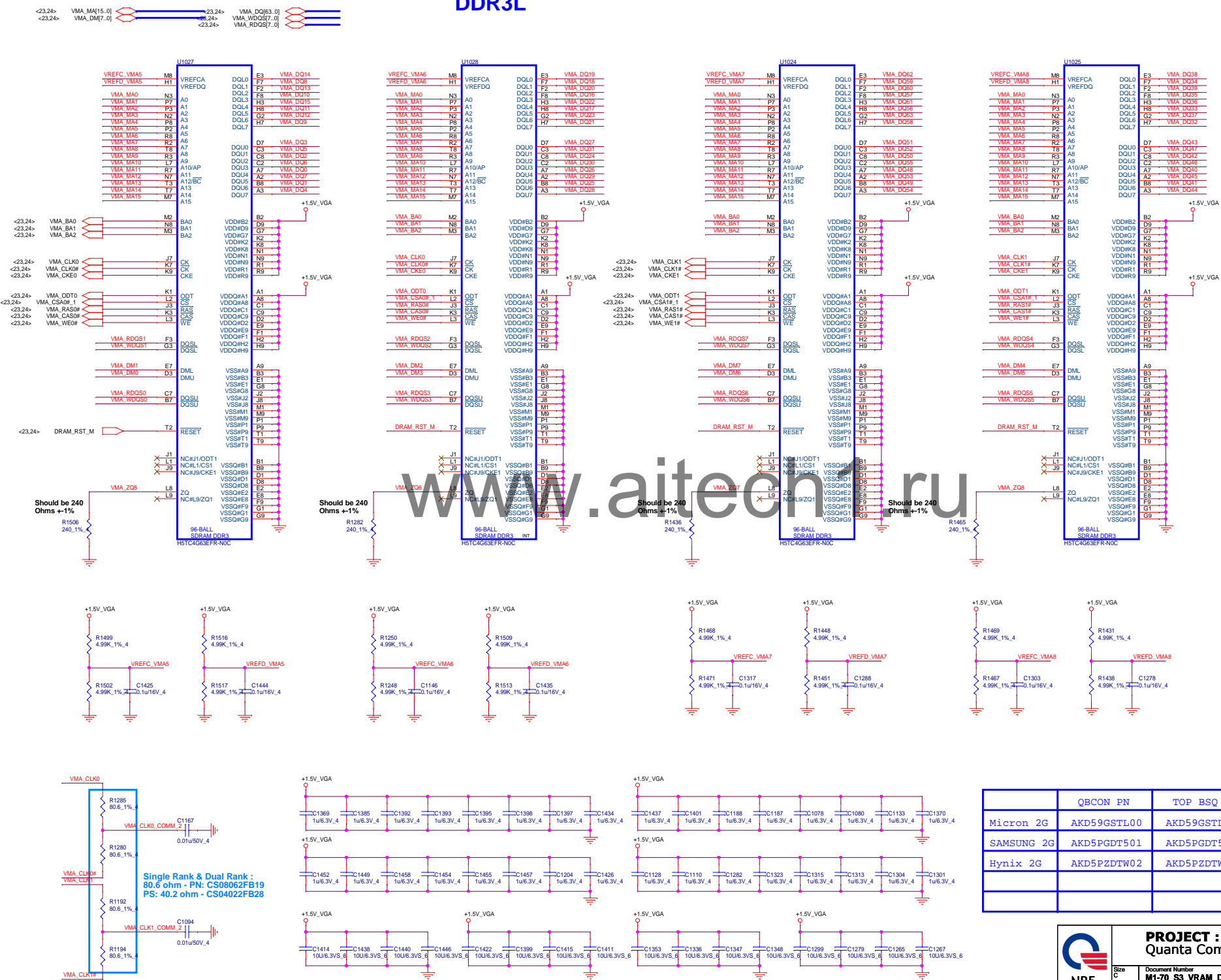
MEMORY INTERFACE



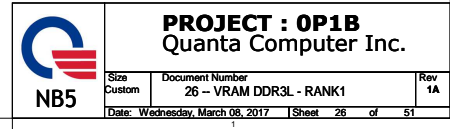
PROJECT : 0P1B
Quanta Computer Inc.

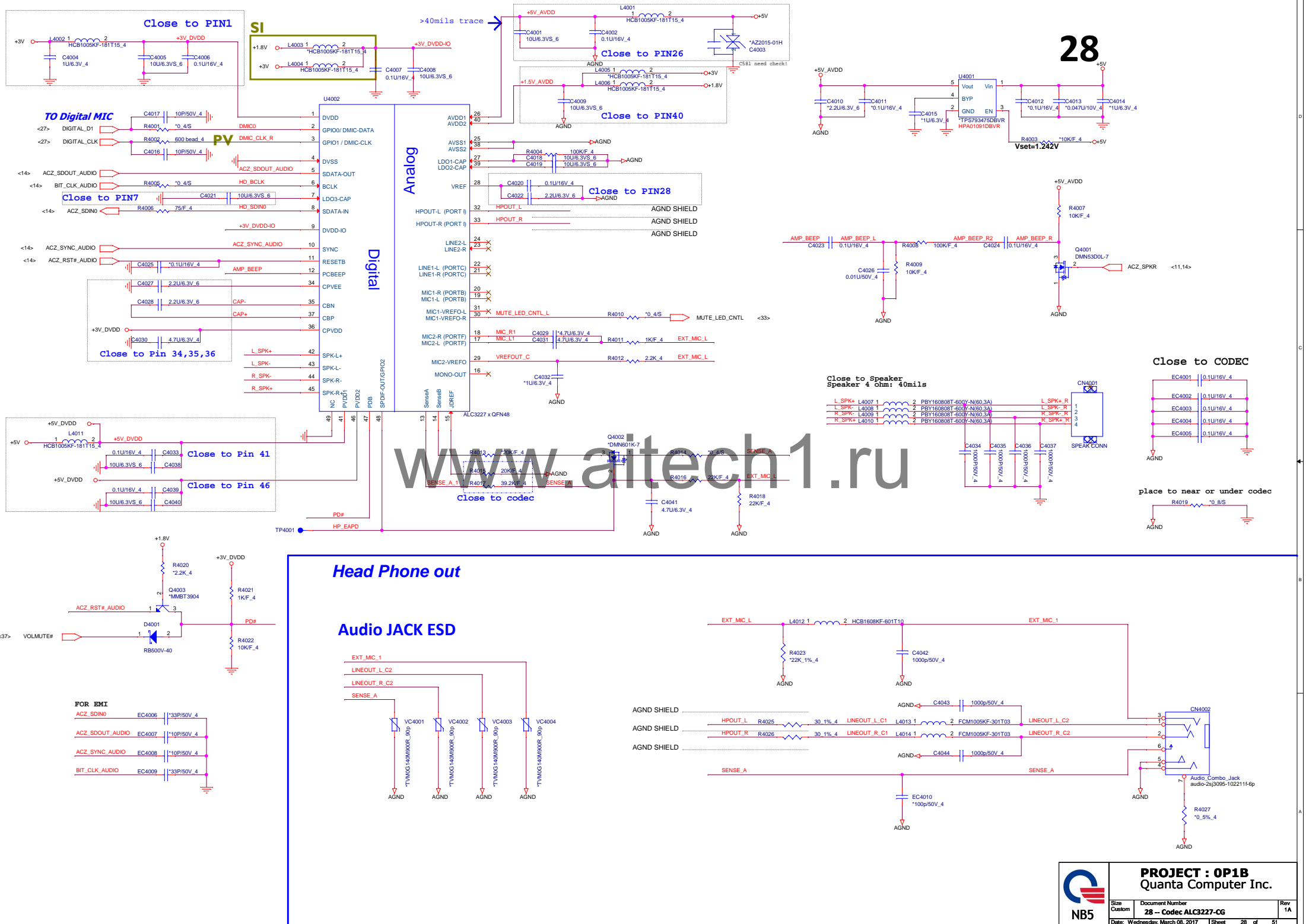
Size	Document Number	Rev
	M1-70_S3_MEM	1A
Date:	Wednesday, March 08, 2017	Sheet 23 of 51





	QBCON PN	TOP BSQ
Micron 2G	AKD59GSTL00	AKD59GSTL01
SAMSUNG 2G	AKD5PGDT501	AKD5PGDT500
Hynix 2G	AKD5PZDTW02	AKD5PZDTW01

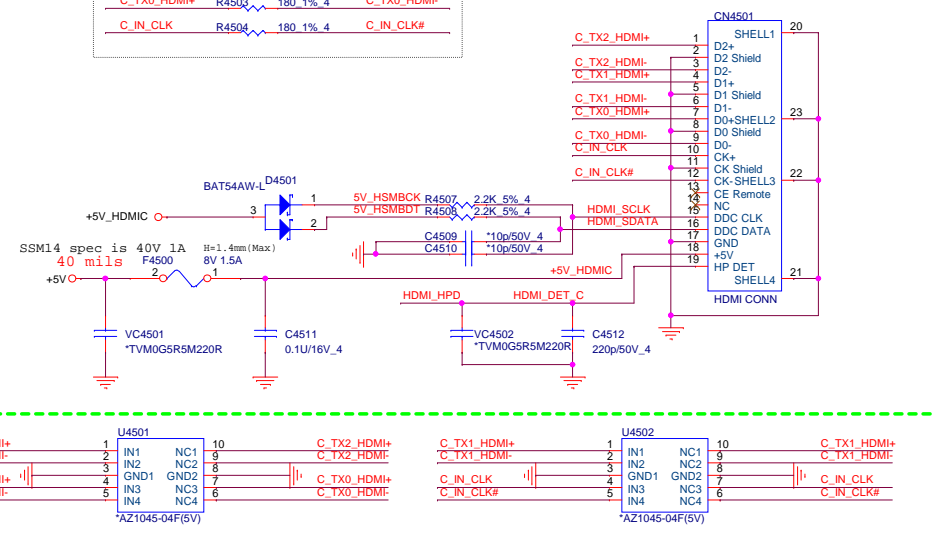
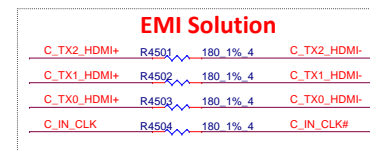
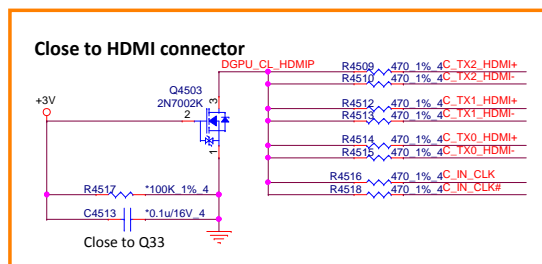
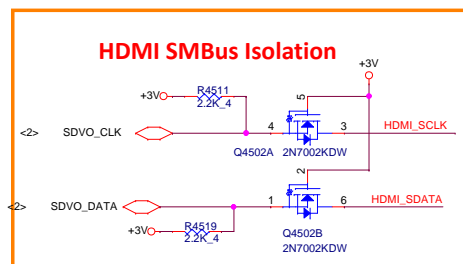
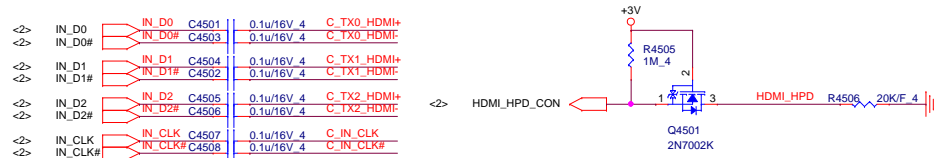




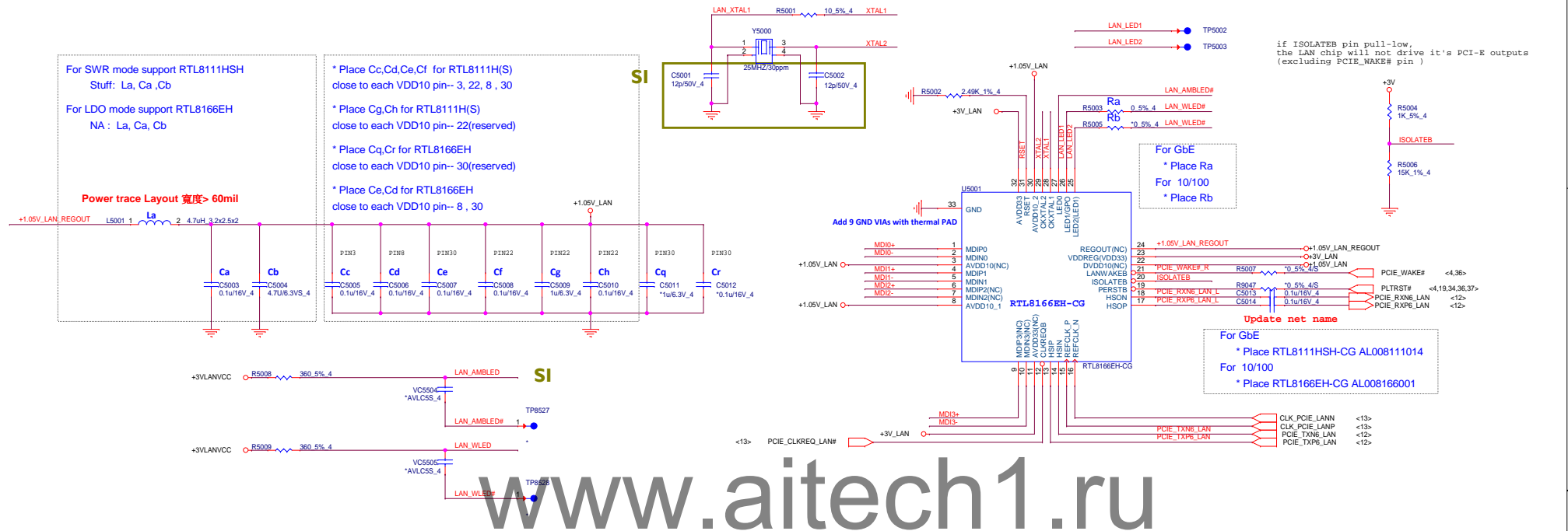
28

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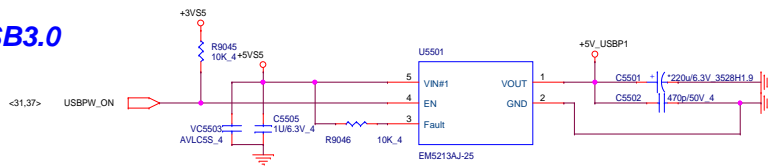
HDMI CONN



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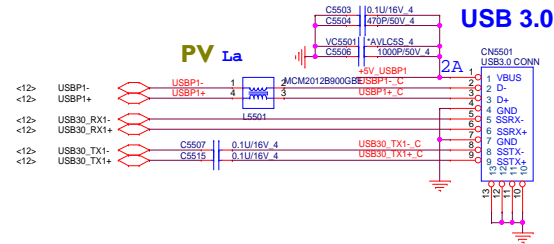
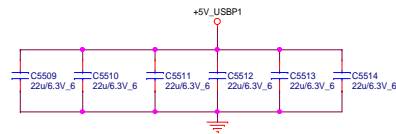
USB3.0



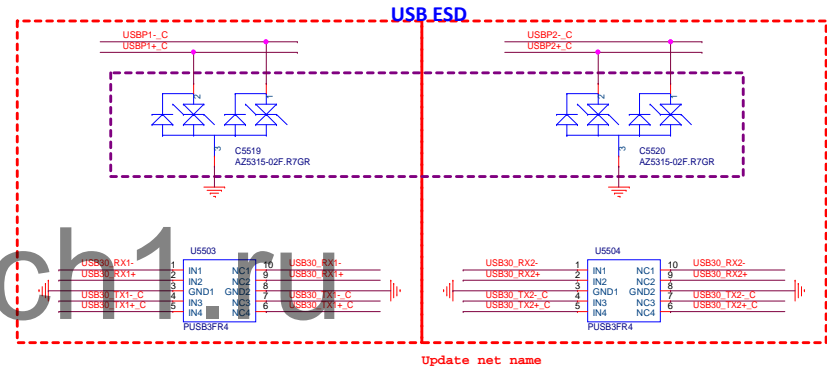
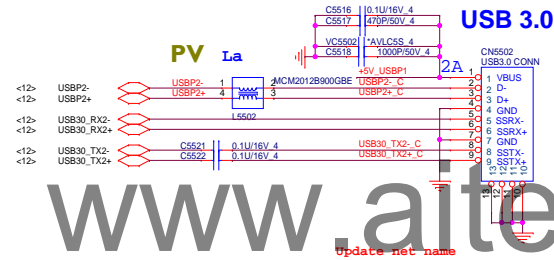
USB 2.0/3.0 Combo

UART for Win7 WHQL DEBUG

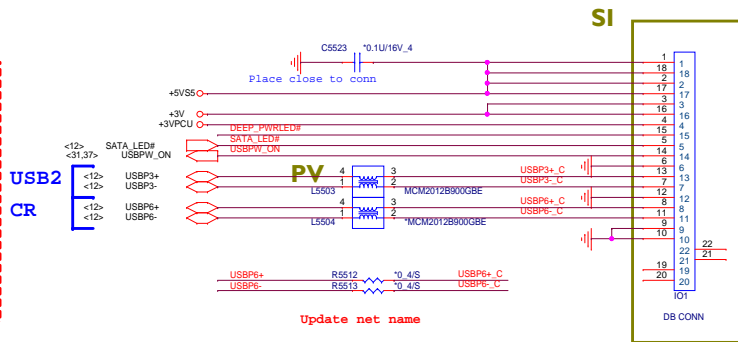
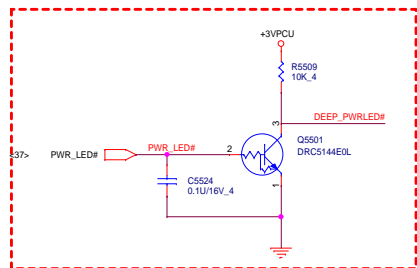
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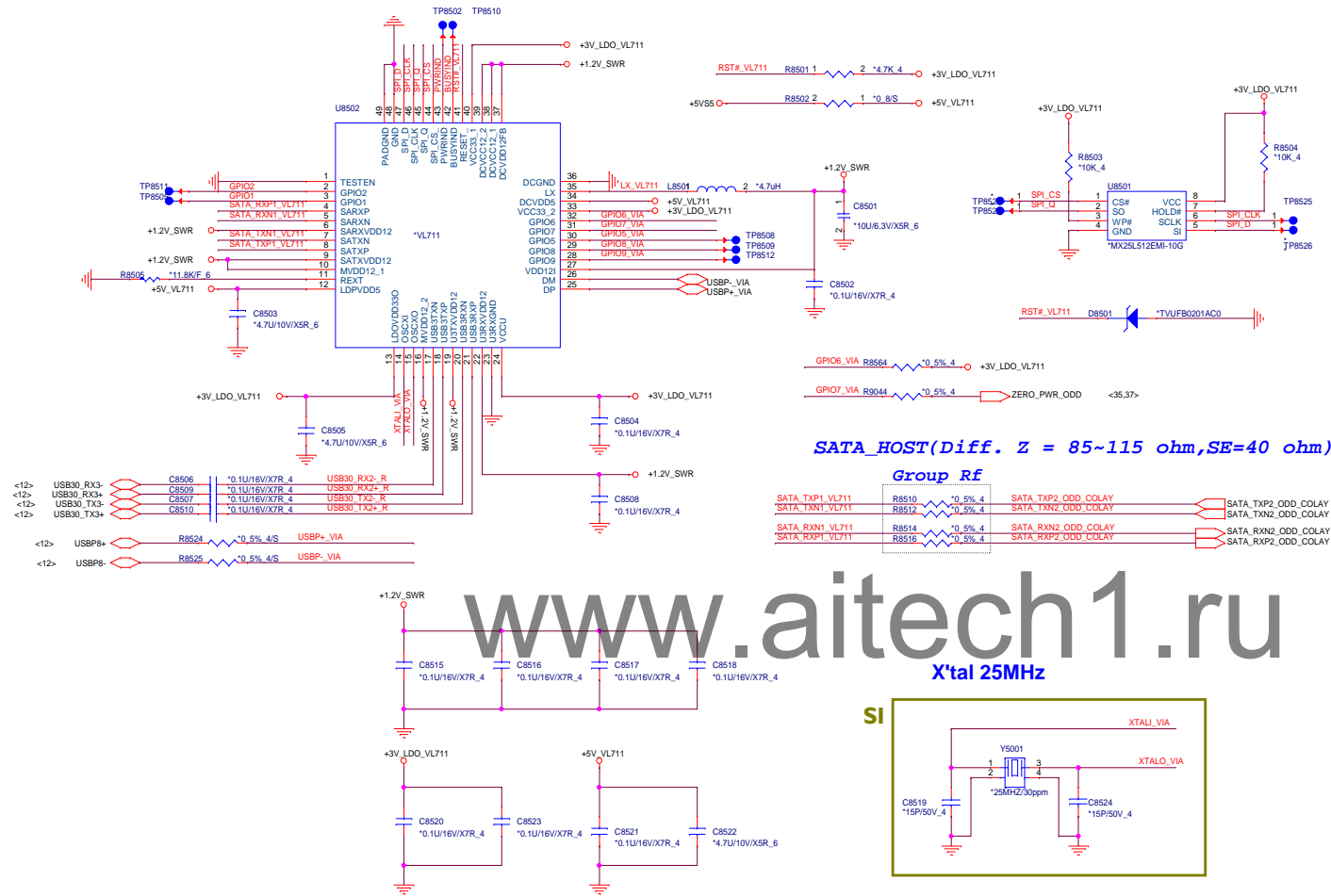


USB 2.0/3.0 Combo

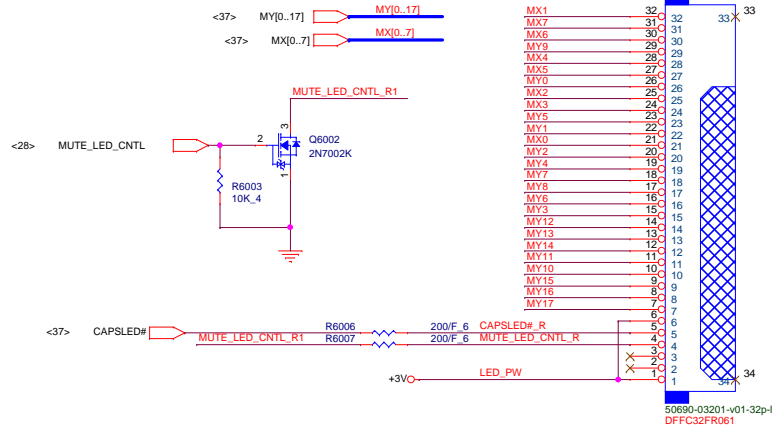


Daughter Board

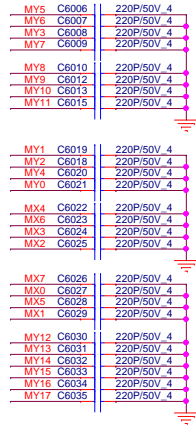
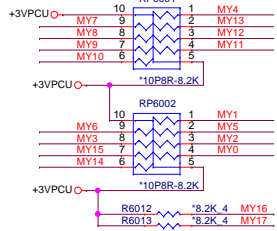




KEYBOARD Con.

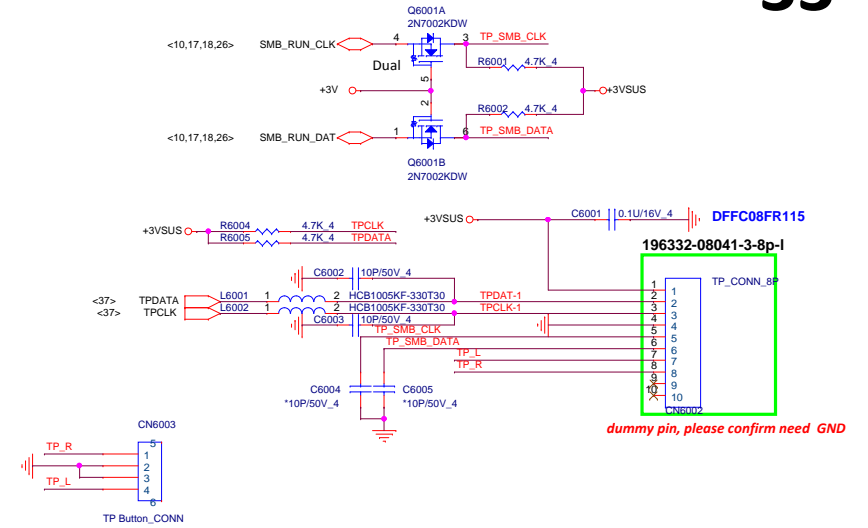


KEYBOARD PULL-UP

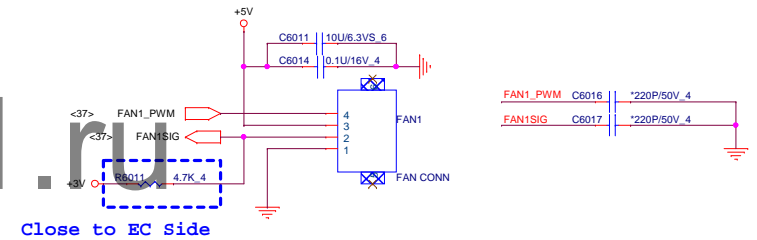


Touch Pad Connector

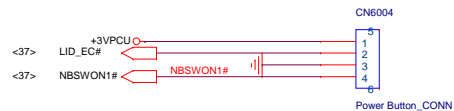
33



FAN

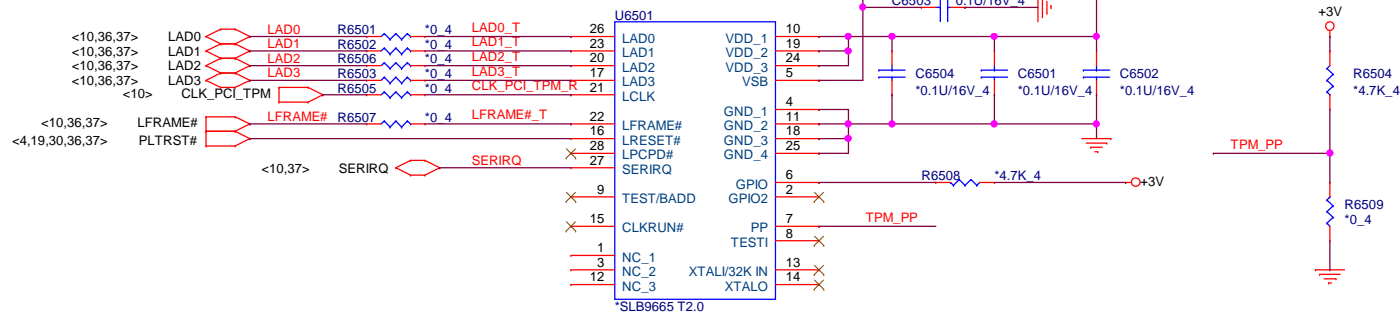


Power Button

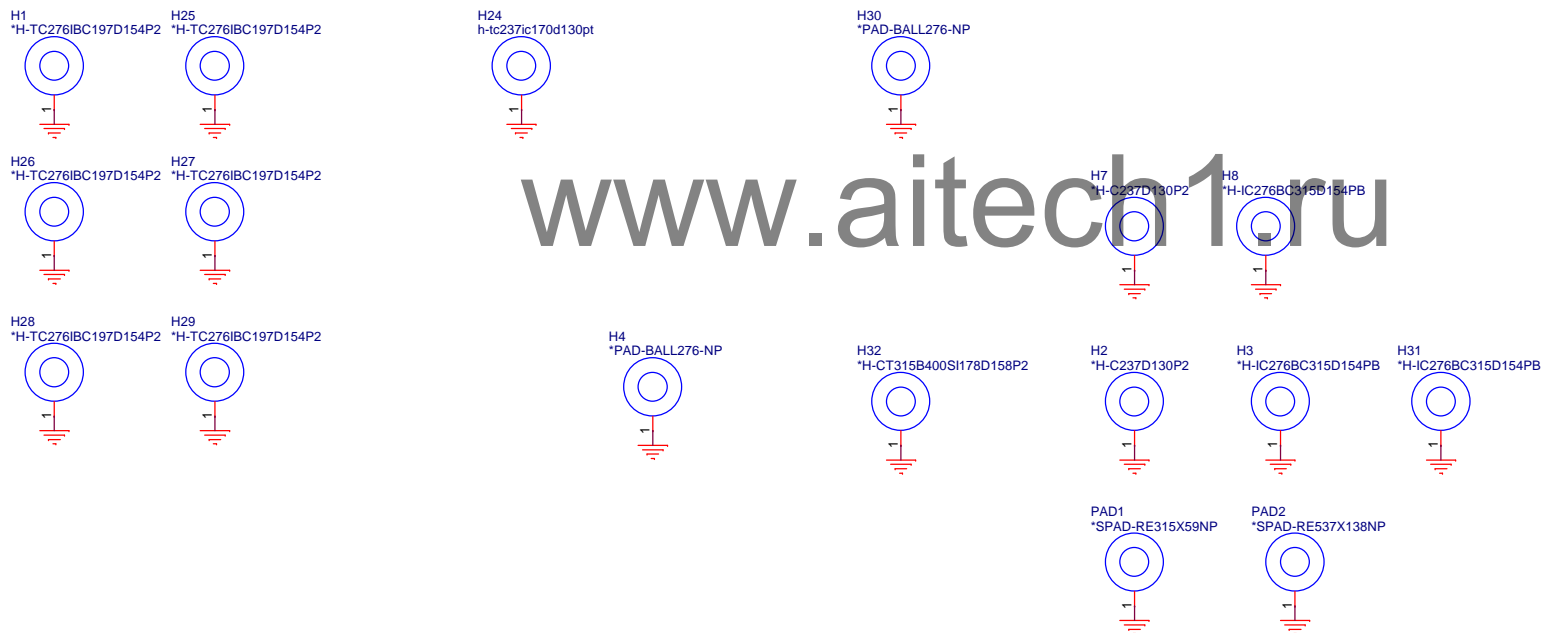


TPM (2.0)

PN:AL009665K05



34



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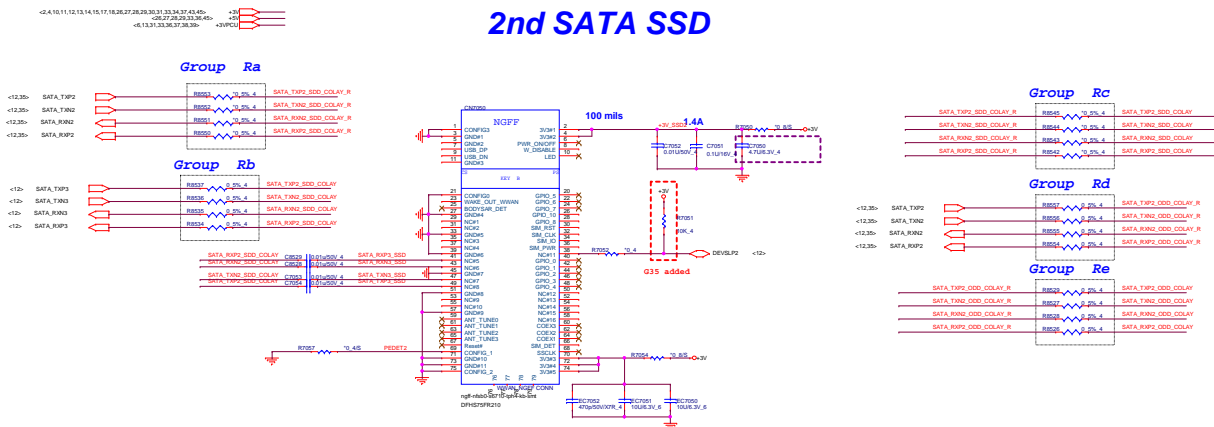


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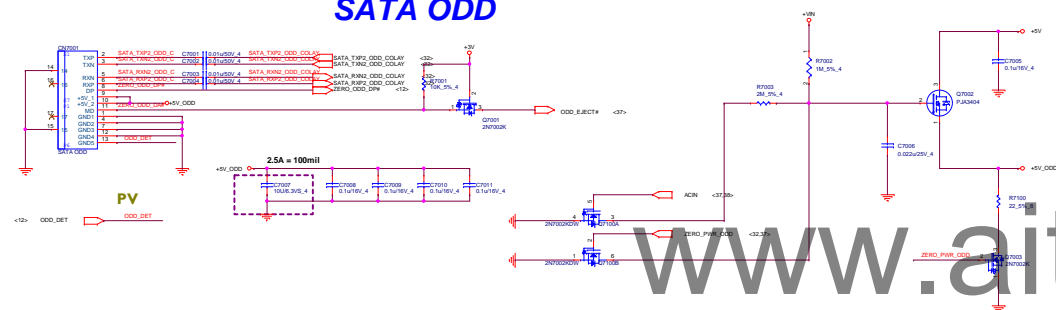
Size	Document Number	Rev
B	34 -- TPM/G-Sensor/IR CAM	1A
Date: Wednesday, March 08, 2017	Sheet	34 of 51

2nd SATA SSD

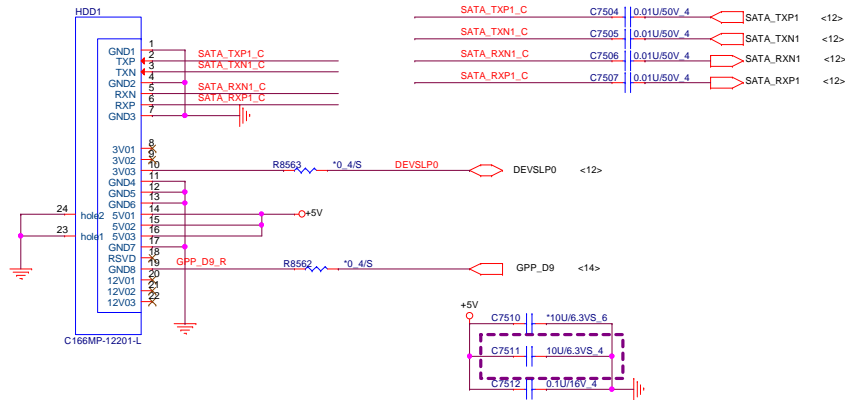
35



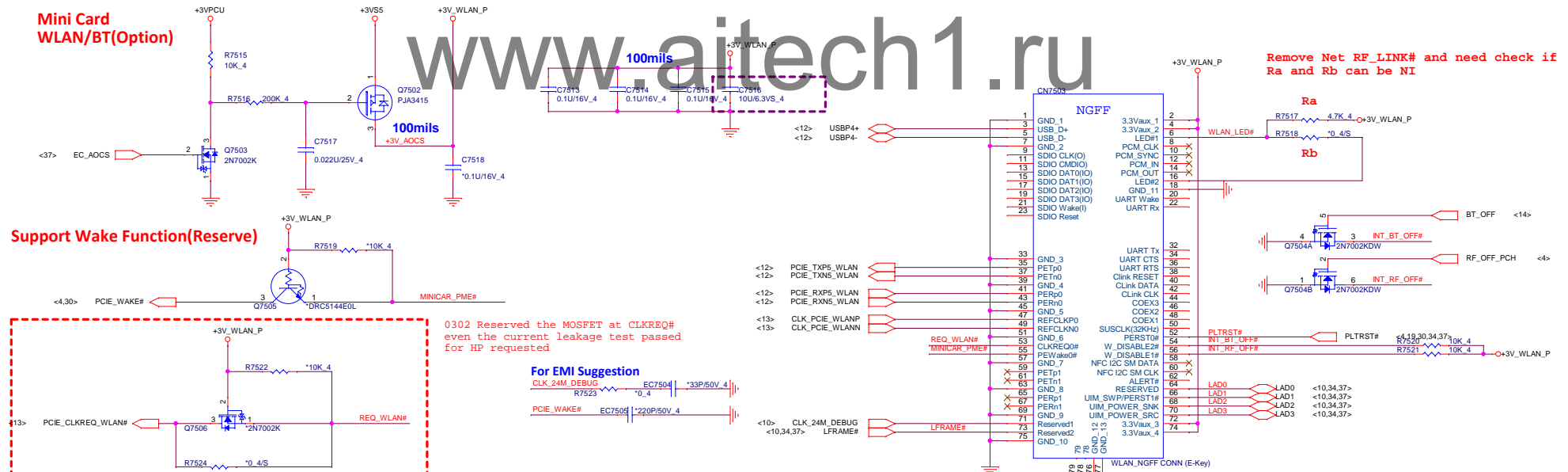
SATA ODD

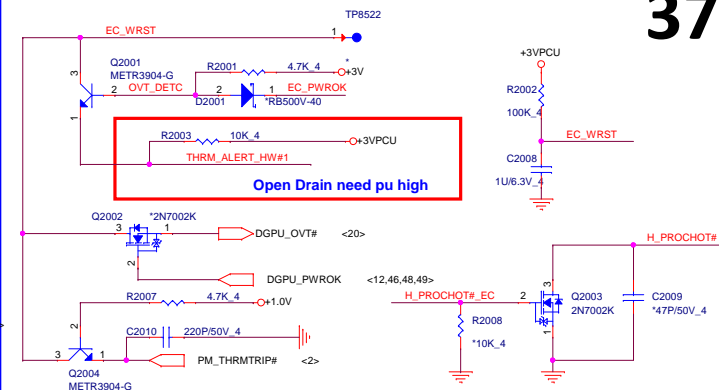
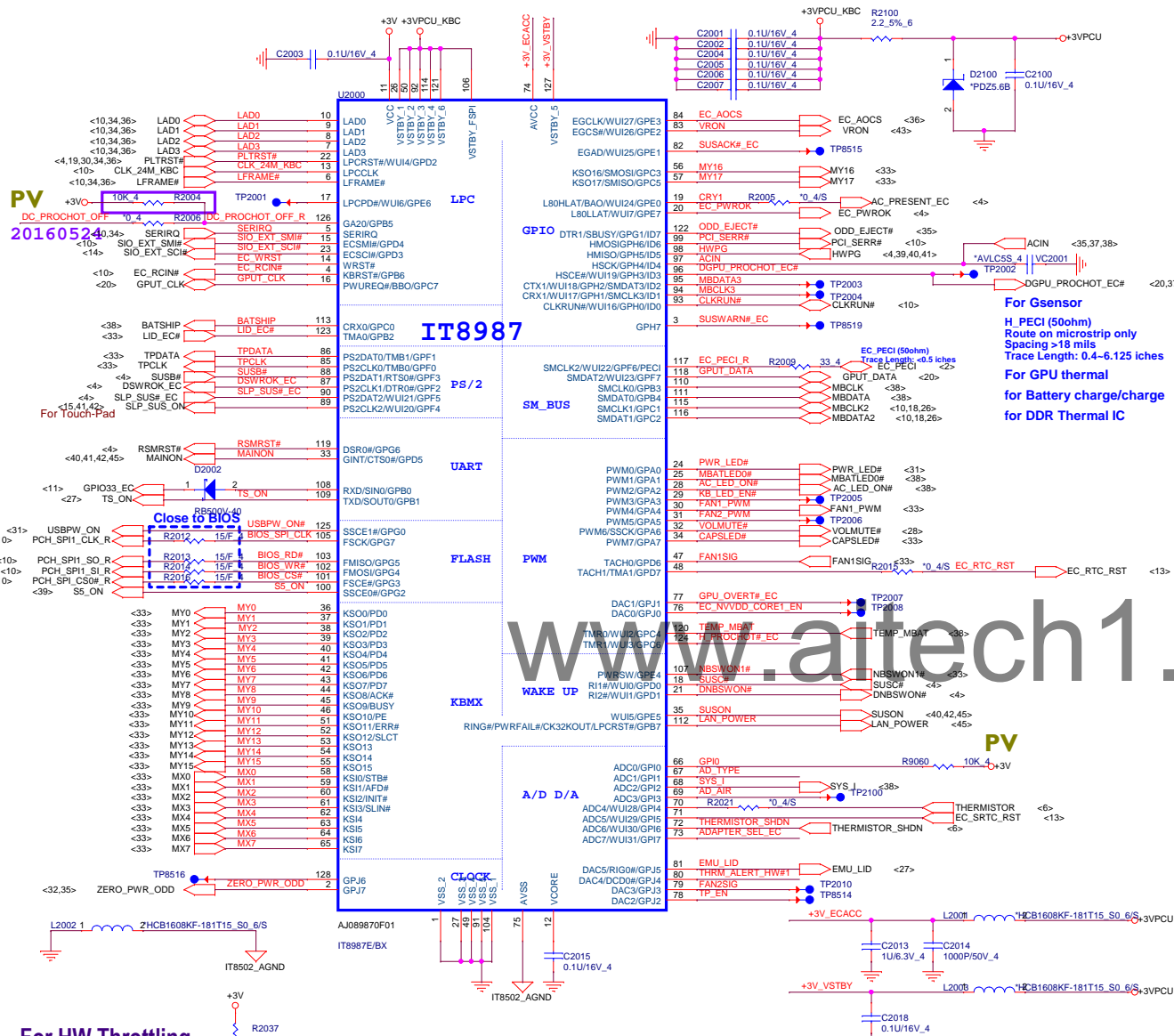


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WLAN

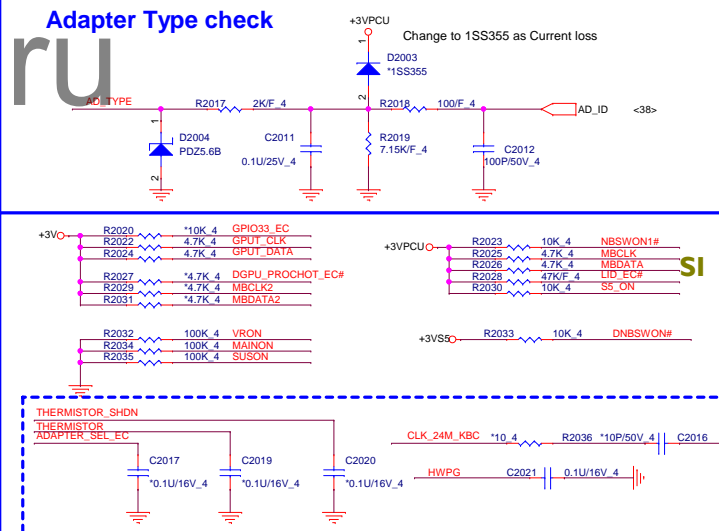




Adapter select for EC

	Ra	Rb	ADAPTER_SEL_EC	BOM
150W	10K(CS31002FB26)	100K(CS41002FB28)	3V	
120W	10K(CS31002FB26)	21.5K	2.25V	
90W	10K(CS31002FB26)	8.33K	1.5V	
65W	10K(CS31002FB26)	2.94K(CS22942FB01)	0.75V	DIS
45W	NC	10K(CS31002FB26)	0V	UMA

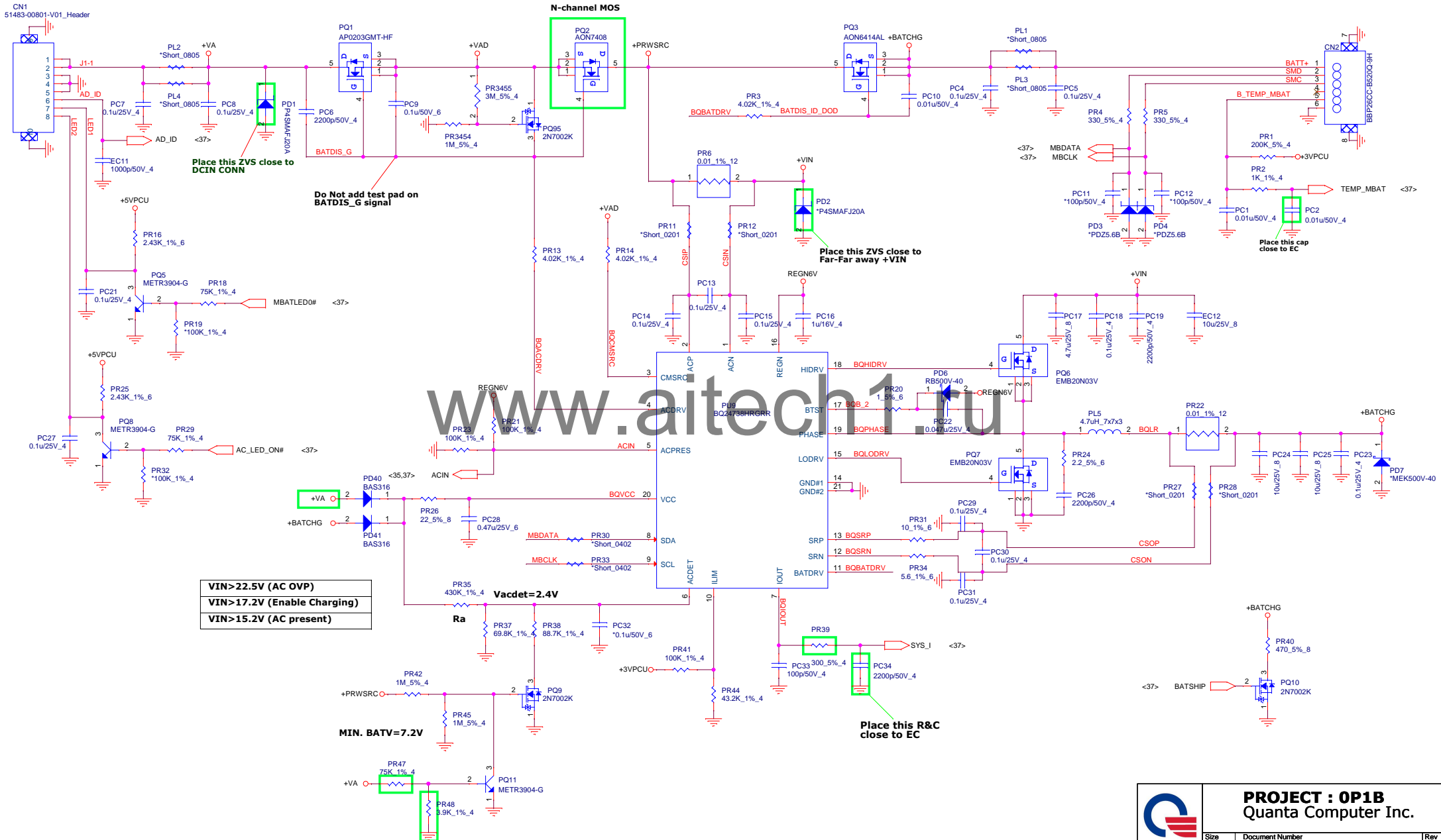
Adapter Type check



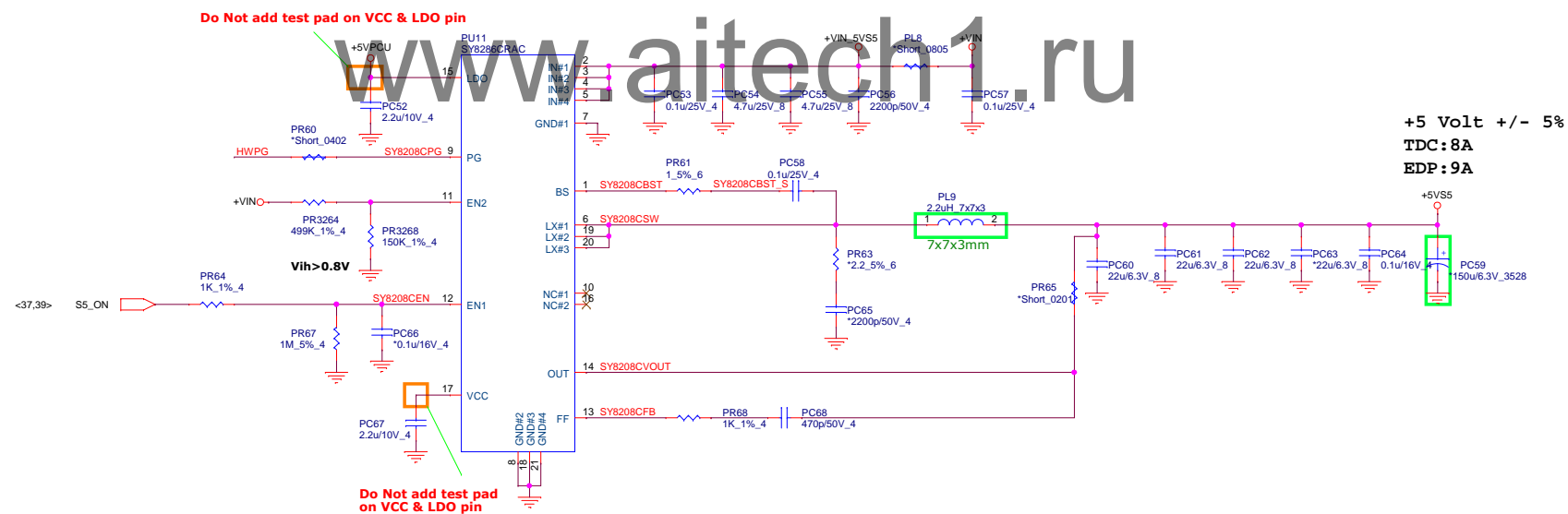
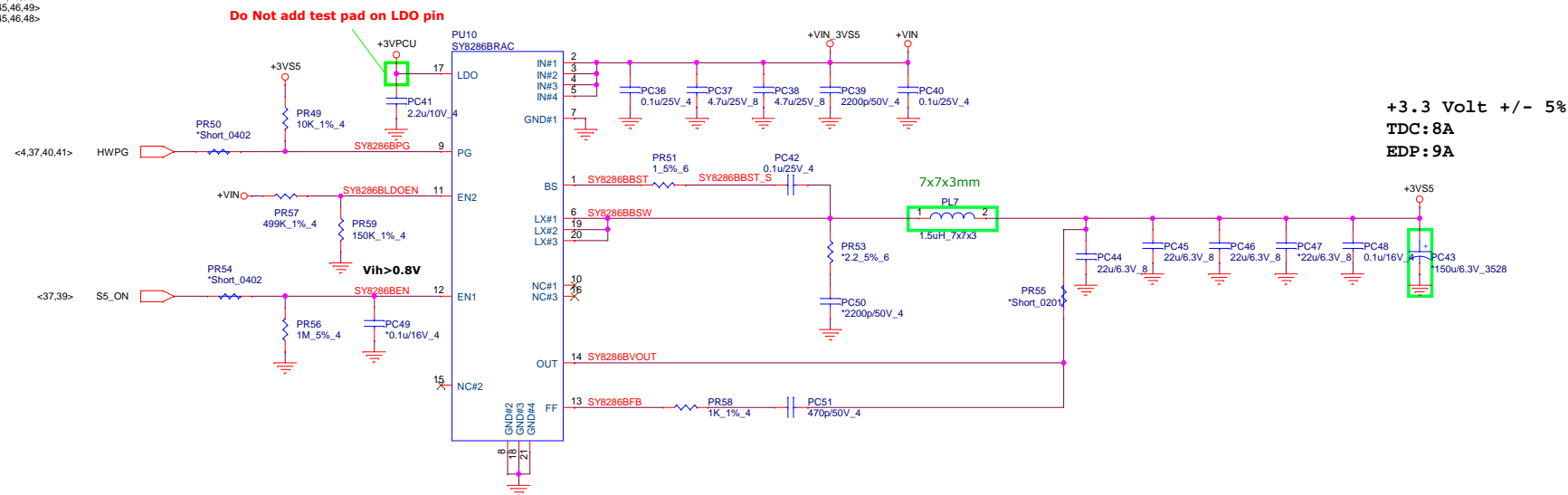
CLOSE to EC Pin

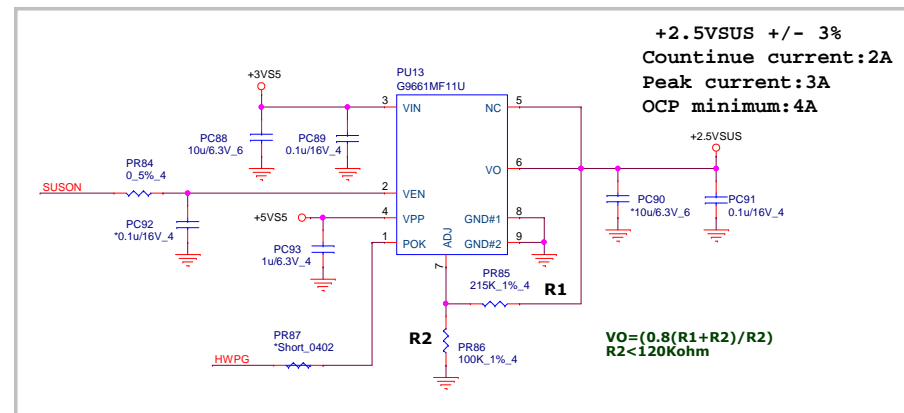
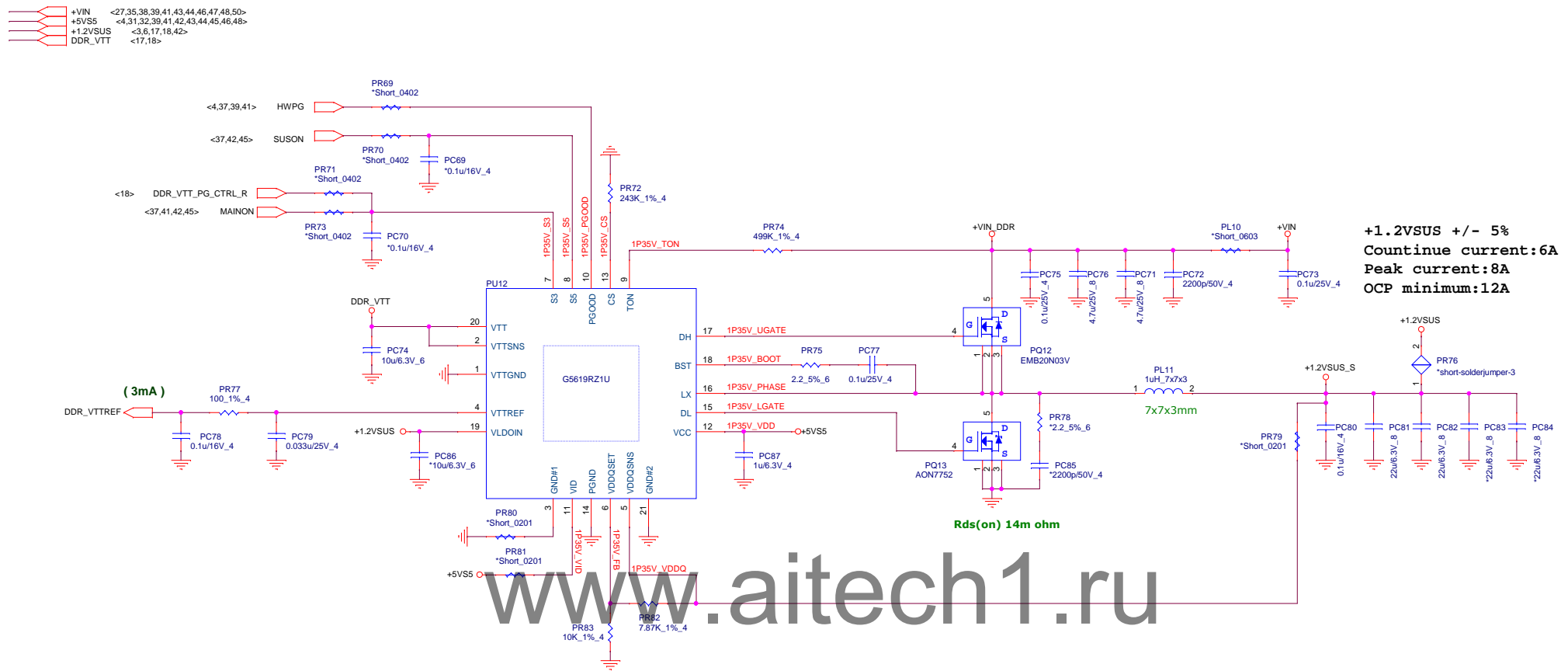
	AC_PRESENT_EC	H_PROCHOT#_EC	H_PROCHOT#
> AC IN: AC mode Operation	H	L	H
AC remove: AC mode to DC mode	L	L	L
DC mode recover from PROCHOT	L	H	H

ADP=65W

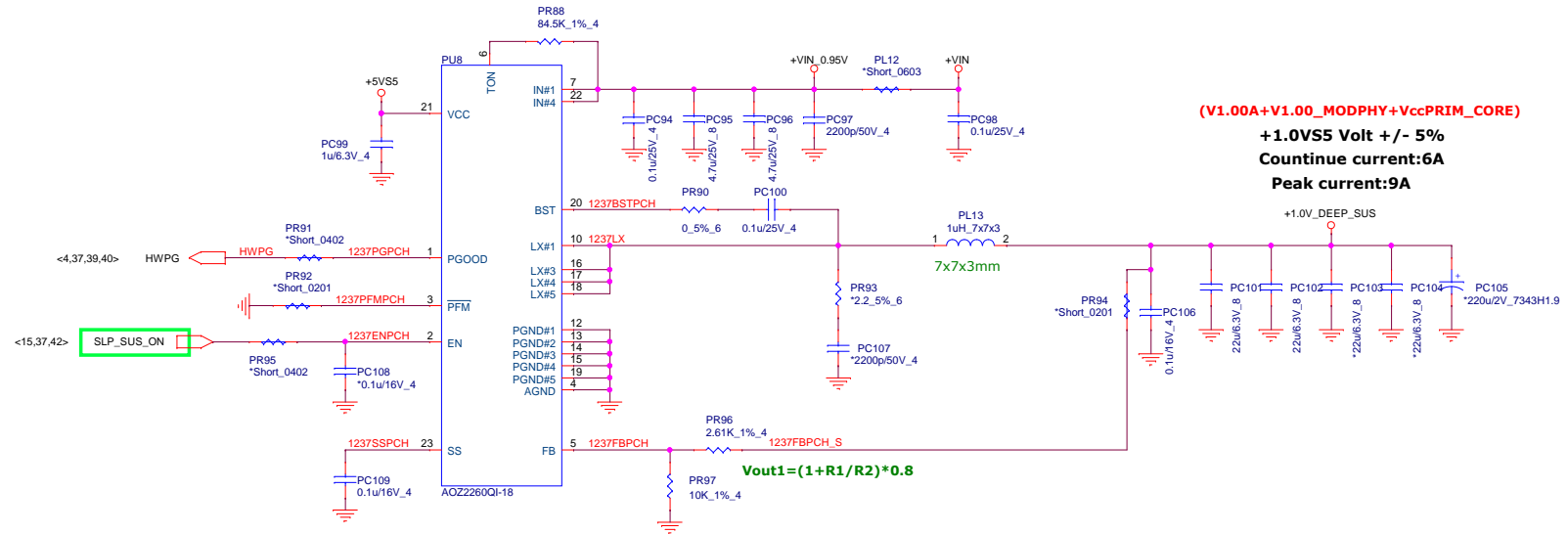


+VIN <27,35,38,40,41,43,44,46,47,48,50>
 +3VS5 <4,15,31,36,37,40,41,42,45,46,49>
 +5VS5 <4,31,32,40,41,42,43,44,45,46,49>
 +3VPCU <6,13,31,33,36,37,38>
 +5VPCU <38,45,49>

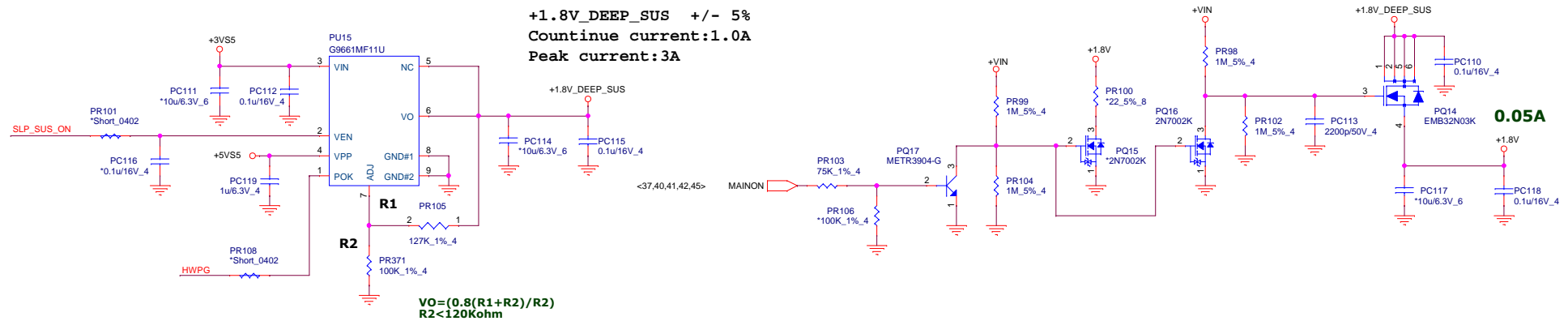




+VIN <27,35,39,39,40,43,44,46,47,48,50>
 +3VS5 <4,15,31,36,37,39,40,42,45,46,49>
 +5VS5 <4,31,32,39,40,42,43,44,45,46,48>
 +1.0V_DEEP_SUS <9,13,15,42>
 +1.8V_DEEP_SUS <9,15,49>
 MAINON <37,40,41,42,45>
 +1.5V



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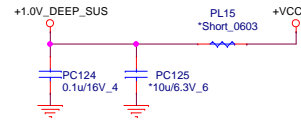


+1.0V	<2,4,37,43>
+3VSS	<4,15,31,36,37,39,40,41,45,46,49>
+5VSS	<4,31,32,39,40,41,43,44,45,46,48>
+VCCIO	<2,6>
+1.2VSUS	<3,6,17,18,40>
+VCCSTPLL	<2,4,5,6,9>
+1.0V_DEEP_SUS	<9,13,15,41>
+1.2V_VCCPLL_OC	<6>
MAINON	<37,40,41,45>

Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

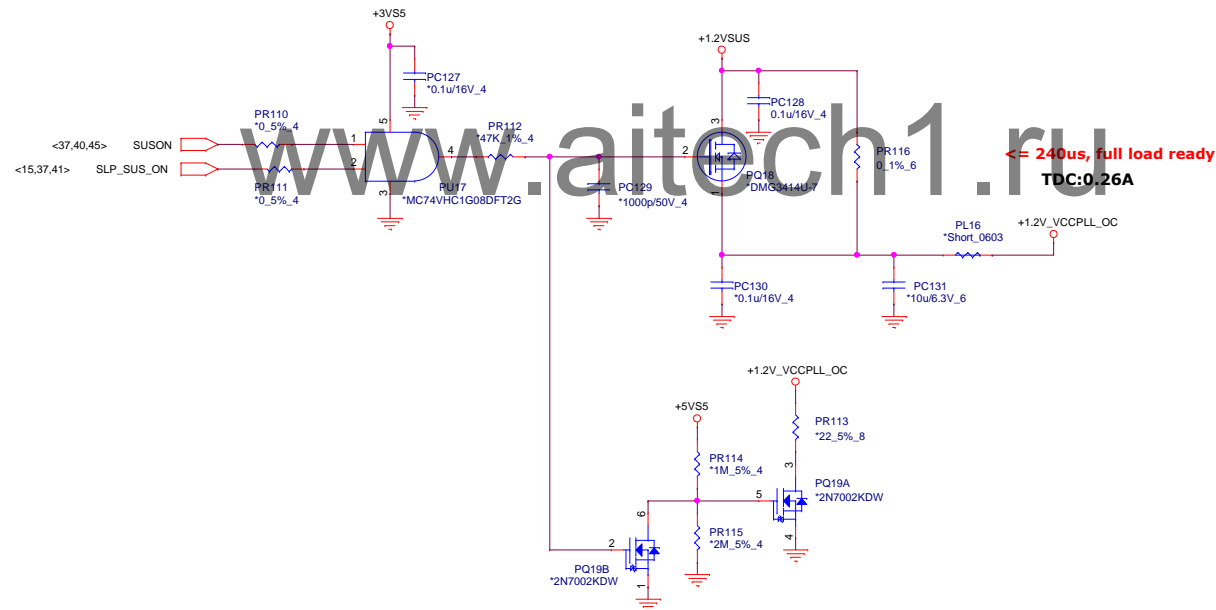
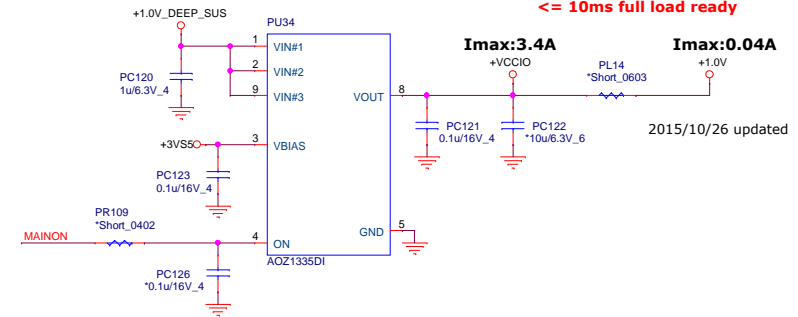
<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)

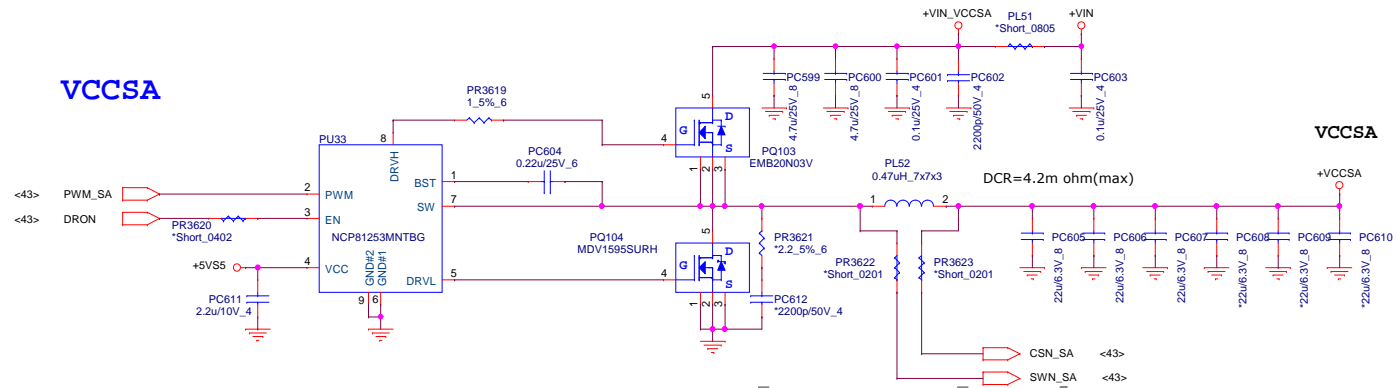
Imax:0.24A



Volume Segment
Vcc_STG: 0.04A
Vcc_IO: 3.4A

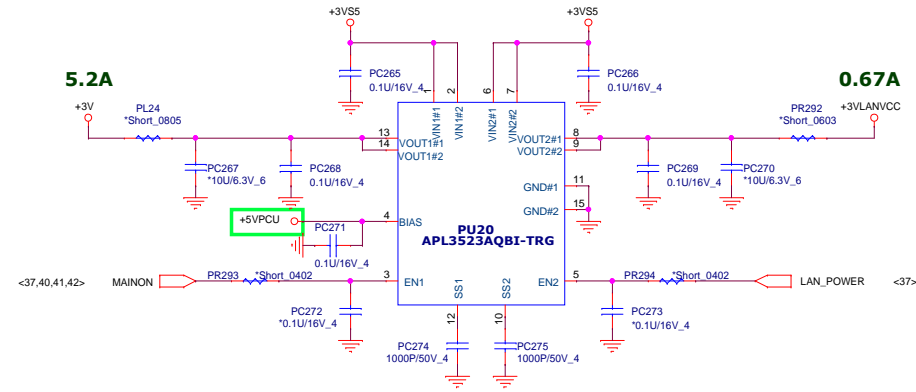
<= 10ms full load ready



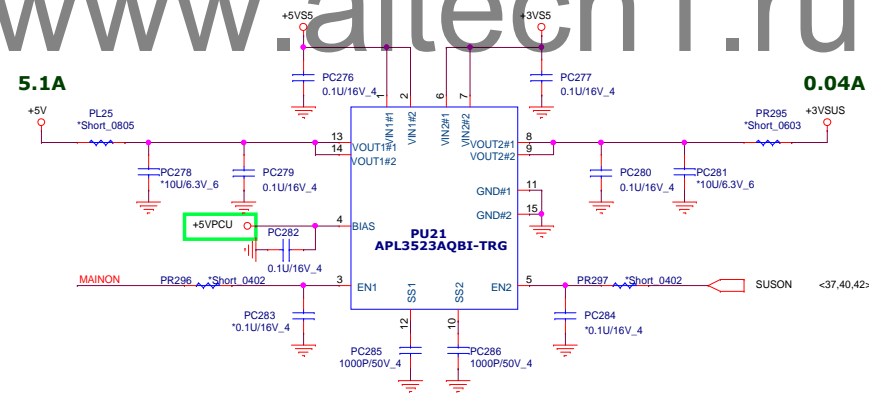


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+3V	<2,4,10,11,12,13,14,15,17,18,26,27,28,29,30,31,33,34,35,37,43>
+5V	<26,27,28,29,33,35,36>
+VIN	<27,35,38,39,40,41,43,44,46,47,48,50>
+3VS5	<4,15,31,36,37,39,40,41,42,46,49>
+5VS5	<4,31,32,39,40,41,42,43,44,46,48>
+3VSUS	<33>
+5VPCU	<38,39,49>
+3VLAVCC	<30>



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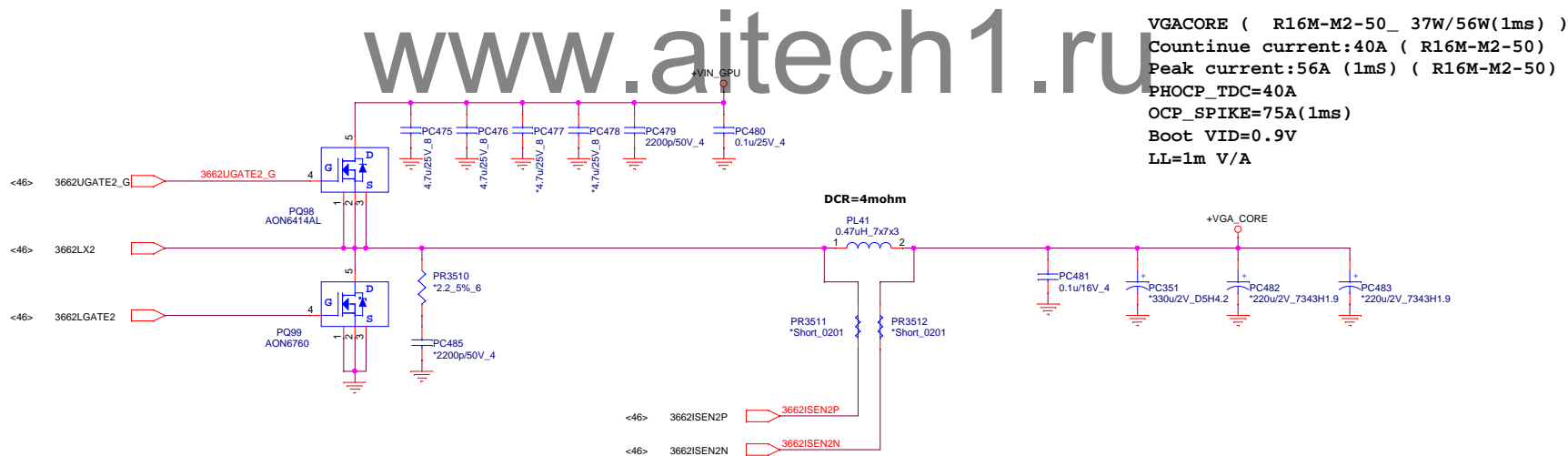
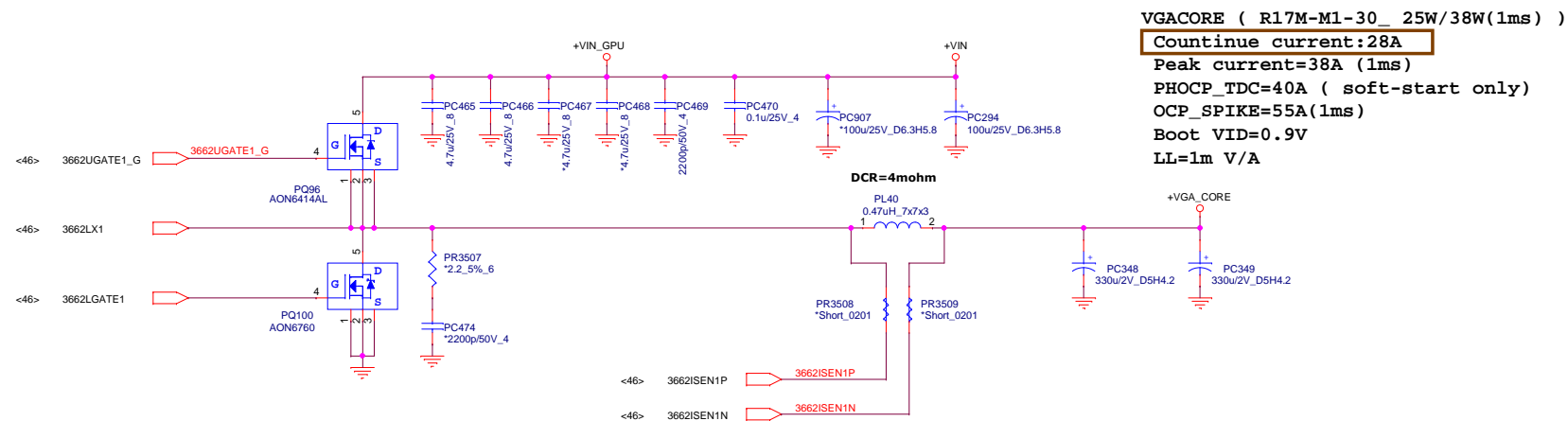
PROJECT : 0P1B
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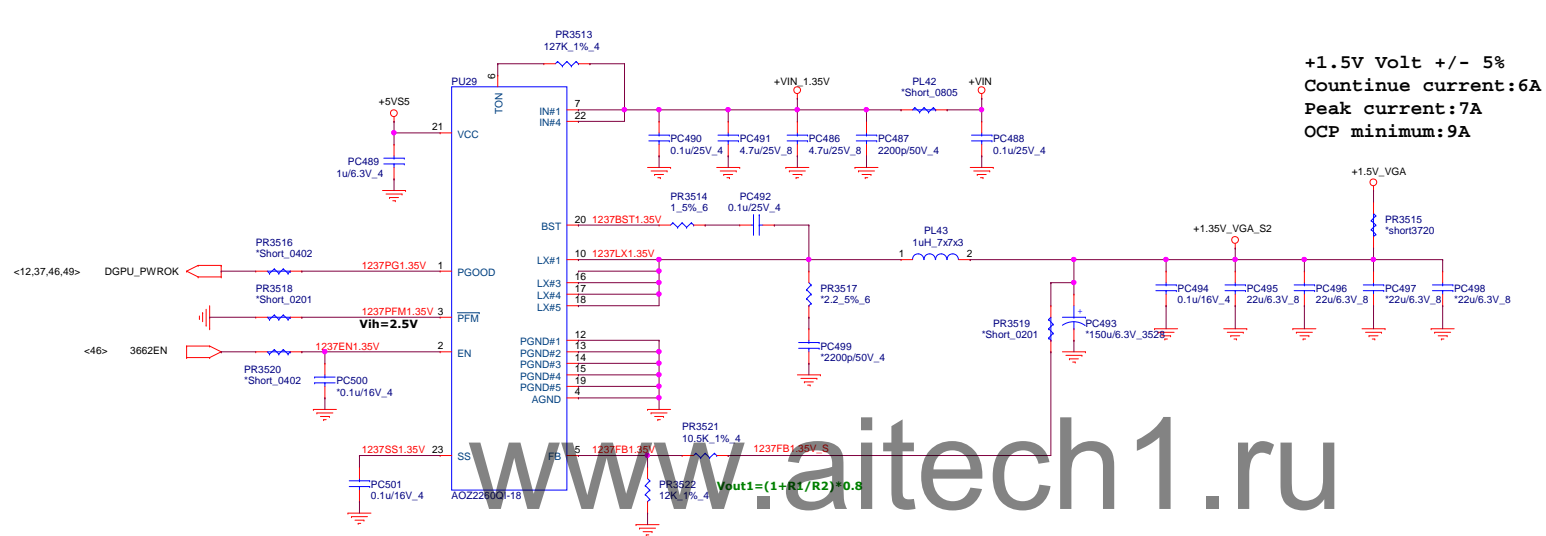
Size Custom	Document Number Load switch IC (APL3523A)	Rev 1A
Date: Wednesday, March 08, 2017	Sheet 45 of 51	

R17M-M1-70

	1 Phase setting	
R1		
R2		
R3		

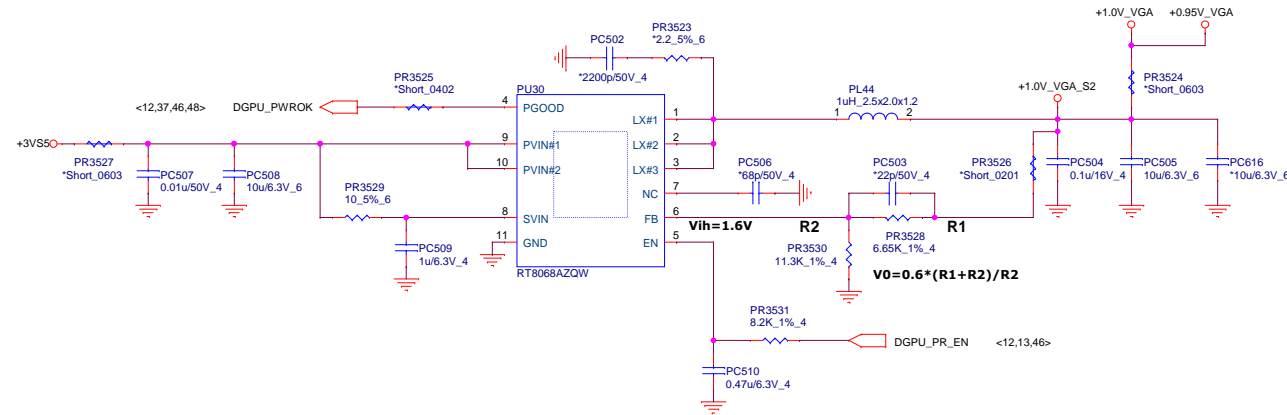
	1 Phase setting	
R4		



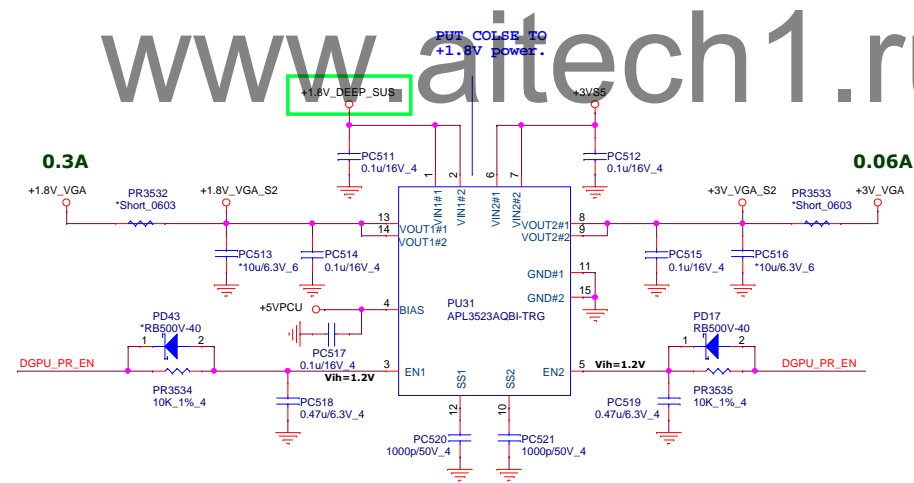


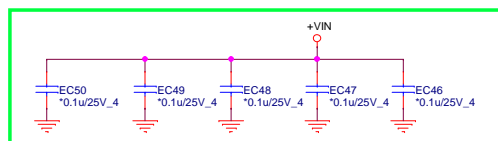
Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

+0.95V +/- 3%
 Countinue current:2A
 Peak current:3A
 OCP minimum:4A

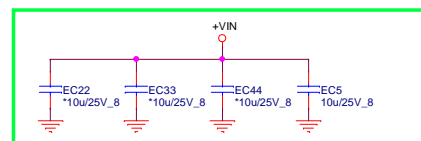


+3V_VGA
 +1.8V_VGA & +0.95V_VGA
 +VGA_CORE & +1.5_VGA

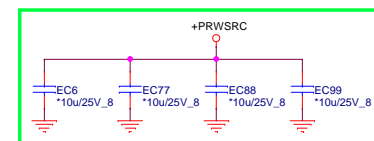




EMI request for ISN




EMI request for ISN



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 NB5	PROJECT : 0P1B Quanta Computer Inc.			
	Size Custom	Document Number EC ENE KB9027B		Rev 1A
	Date: Wednesday, March 08, 2017		Sheet	51 of 51